A CAPACITOR-FREE LOW DROPOUT REGULATOR FOR LOW POWER SYSTEM-ON-CHIP APPLICATIONS

Oscar Igor Robles Palacios

Dissertação de Mestrado apresentada ao Programa de Pós-graduação em Engenharia Elétrica, COPPE, da Universidade Federal do Rio de Janeiro, como parte dos requisitos necessários à obtenção do título de Mestre em Engenharia Elétrica.

Orientador: Antonio Petraglia

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Examinada por:

Prof. Antonio Petraglia, Ph.D.

Prof. Antonio Carneiro de Mesquita Filho, Dr.d'État

Prof. Marcio Nogueira de Souza, D.Sc.

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Palacios, Oscar Igor Robles

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"Para odiar hay que querer
para destruir hay que hacer
y estoy orgulloso
de quererte romper
la cabeza contra la pared
Para dejar hay que beber
para morir primero
hay que nacer
siento ganas nuevamente
de tirarme a tus pies
y llevarte a mi morada otra vez
Si lo sembrás lo recogés
y si esperás vas a entender
cuando las cosas salen
como no las espero
la vida me hace más guerrero."
Intoxicados - Nunca Quise

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A CAPACITOR-FREE LOW DROPOUT REGULATOR FOR LOW POWER SYSTEM-ON-CHIP APPLICATIONS

Oscar Igor Robles Palacios

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Orientador: Antonio Petraglia

Programa: Engenharia Elétrica

Low-dropout regulators (LDOs) são importantes blocos de gerenciamento de energia dentro de qualquer sistema eletrônico. Eles são responsáveis pela geração de uma fonte estável e livre de espúrias, o que é especialmente crítico quando se trabalha com circuitos sensíveis ao ruído. Para aplicações de *System on Chip* (SoC), onde o uso da área e o consumo de energia devem ser otimizados, os LDOs aparecem como uma opção eficiente para a geração de energia limpa devido à sua estrutura relativamente simples e a necessidade de poucos componentes externos. Os principais objetivos no projeto de LDO são minimizar o consumo de corrente quiescente e evitar o uso de capacitores externos e, simultaneamente, conseguir estabilidade elevada, regulação precisa e uma rápida resposta. Nesta dissertação, várias técnicas - tais como *dynamic biasing*, *active feedback* e *slew rate enhancement* - são revistas e aplicadas à estrutura básica de um LDO a fim de atingir os objetivos acima mencionados. O circuito foi implementado utilizando um processo CMOS 180nm. O LDO é desenvolvido para fornecer 1.8 V para uma carga máxima de 50 mA, com um *dropout* mínimo de 200 mV e uma corrente quiescente máxima de 58 μA. O LDO projetado é estável em qualquer situação, mesmo quando nenhuma carga está presente, assumindo uma capacidade de carga máxima de 50 pF. Uma rejeição da fonte de alimentação máxima de -40 dB @ 10 kHz é assegurada. O *overshoot* e *undershoot* são menores do que 200 mV para mudanças de carga completa dentro de 1 μs, e o tempo de recuperação é inferior a 3 μs.

Abstract of Dissertation presented to COPPE/UFRJ as a partial fulfillment of the requirements for the degree of Master of Science (M.Sc.)

A CAPACITOR-FREE LOW DROPOUT REGULATOR FOR LOW POWER SYSTEM-ON-CHIP APPLICATIONS

Oscar Igor Robles Palacios

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Advisor: Antonio Petraglia

Department: Electrical Engineering

Low-dropout regulators (LDOs) are key power management blocks within any electronic system. They are in charge of generating a spurious free and stable supply, which is critical specially when working with noise sensitive circuits. For System on Chip (SoC) applications, where area usage and power consumption are to be optimized, LDOs appear as an efficient option for clean supply generation due to their relatively simple structure and few external components. The main objectives in LDO design are the minimization of the quiescent current consumption and the avoidance of external capacitors, while achieving high stability, accurate regulation and fast response. In this dissertation, several techniques - such as, dynamic biasing, active feedback, and slew rate enhancement - are reviewed and applied to the basic structure of an LDO in order to attain the aforementioned goals. The circuit was implemented using a 180nm CMOS process. The developed LDO supplies $1.8V$ to a maximum load of 50 mA, with a minimum dropout of 200 mV and a maximum quiescent current of 58 μA. The designed LDO is stable in any scenario, even when no load is present, assuming a maximum load capacitance of 50 pF. A maximum power supply rejection of -40 dB @ 10 kHz is ensured. The maximum overshoot and undershoot are less than 200 mV for full load current changes in 1 μs, and the recovery time is less than 3 μs.

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List of Acronyms

ASIC	Application-Specific Integrated Circuit, p. 2
CAD	Computer-Aided Design, p. 56
CMOS	Complementary Metal-Oxide Semiconductor, p. 1
EA	Error Amplifier, p. 5
EM	Electromigration, p. 51
ESR	Equivalent Series Resistance, p. 5
FVF	Flipped Voltage Follower, p. 10
GBW	Gain-Bandwidth, p. 46
ICMR	Input Common-Mode Range, p. 9
LDO	Low-Dropout Regulator, p. vii
LHP	Left-Hand Plane, p. 6
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor, p. 11
OLG	Open-Loop Gain, p. 7
Op-Amp	Operational Amplifier, p. 5
OTA	Operational Transconductance Amplifier, p. 7
PDK	Process Design Kit, p. 47
PM	Phase Margin, p. 17
PSRR	Power Supply Rejection Ratio, p. 1
RC	Resistance-Capacitance, p. 20
RHP	Right-Hand Plane, p. 7

SoC	System on Chip, p. vii
SR	Slew Rate, p. 8
SRE	Slew Rate Enhancement, p. 29
UGF	Unity Gain Frequency, p. 2

Chapter 1

Introduction

This work intends to show the entire design - up to the physical implementation using a 180 nm CMOS (Complementary Metal Oxide Semiconductor) process - of an LDO that presents high stability, high PSRR (Power Supply Rejection Ratio), and a fast transient response without the usage of any external components, such as capacitors. This LDO is a critical block of power management units, since it is meant to provide a clean and stable voltage supply for all highly sensitive analog circuits within an energy measurement SoC, which is the main application of this work. This type of SoC comprises both digital and analog circuitry, which are in most cases placed inside the die with considerable proximity to each other. Thus, the sensitive analog circuits must be isolated from the noise caused by the switching nature of the digital circuits. Furthermore, due to the necessity to avoid external components, several new techniques are applied to the traditional LDO topology. Hence, this dissertation will focus on the analysis of this new architecture, which mainly consists in the study of its behavior in both the frequency and time domains.

1.1 Motivation

LDOs have been one of the most essential building blocks in any Power Management Unit for quite some time. As a consequence, they have been a vastly popular choice among all sorts of electronic systems, where a stable voltage supply must be guaranteed regardless of any changes in the input voltage supply, current output load, or temperature. Depending on how sudden and significant the changes in both the input supply and output load, most LDOs may require an output capacitor in order to provide a charge/discharge outlet when the LDO is not fast enough to handle the aforementioned variations. Moreover, the output capacitor usually sets the dominant pole and works with an in-series resistor to generate a zero in the frequency response of the loop, which improves both the frequency stability and the PSRR performance of the LDO. However, as in any other field of electronics,

the trend is always to reduce the area usage, which applies to both the die and the board. As new fabrication processes appear, the minimum dimensions get smaller (nano-scale), which allows the electronic industry to demand the same results but inside a much smaller package. Thus, with so many portable applications emerging, output-capacitorless LDOs became a very promising research topic.

As the complexity of the portable applications grows, a SoC, instead of a simple ASIC (Application-Specific Integrated Circuit), appears as a more suitable choice. This, in turn, implies the coexistence of both digital and analog circuits within the same die. As a consequence, the LDO becomes a necessity since analog circuits must be shielded from the noise generated by the switching of the digital signals. Since this noise may have components in the scale of kilohertz as well as megahertz, the LDO must posses a good PSRR performance over a wide frequency range. Moreover, some SoCs can withhold a large circuit density, which derives in the use of not one but several LDOs in order to power up different analog blocks inside the system. This reduces the crosstalk effect and helps to mitigate the load-transient voltage spikes caused by the bonding wire inductors.

Another trend established by this growth of portable applications is the need to reduce the power consumption. Both supply operating voltage and current consumption of the circuits are decreasing rapidly in order to meet this new requisite. The former is a direct consequence of the new fabrication processes, which decrease not only the minimum dimensions, but also the threshold voltage of the transistors, thereby allowing an abatement of the operating supply voltage. The latter is related to the use of batteries as the input supply; the lower the current consumption, the longer the lifetime of the battery. As a result, low voltage and low quiescent current LDOs have become an attractive option for this type of applications.

1.2 Objectives

The purpose of this work is the realization of an output-capacitorless LDO that presents frequency stability for all load conditions, high PSRR performance for a wide frequency range, fast transient response and high current efficiency. Thus, several State-of-the-Art techniques will be studied in order to improve both the frequency and transient responses of the circuit, while reducing the current consumption.

The main goal is to achieve frequency stability even when there is no load present, while also attaining a high unity-gain-frequency (UGF), which has to be at least 1 MHz, specially for high load currents. This becomes a challenge since the LDO must be fully integrated, which means no external capacitor can be used to set the dominant pole of the frequency response. Even though no external capacitor must

be used, there will be a load capacitance generated by the parasitic capacitances of the power distribution metal paths inside the microchip. In this case, the load capacitance is not expected to surpass the 50 pF value. Moreover, achieving the frequency stability specification while maintaining the current consumption at a minimum is not an easy task. Nevertheless, this specification must be met in order to deliver a state-of-the-art LDO.

The idea is to use this LDO to supply every low voltage sub-circuit of the SoC. Thereby, according to the specification of the 180 nm CMOS process, the required supply voltage will be 1.8 V, with a maximum load current of 50 mA. Besides the supply voltage and current load, the PSRR specification is the one that defines the performance of the LDO. The more rejection to the supply noise, the cleaner the output voltage signal, which translates to a better regulation. As mentioned in Section 1.1, the noise present in the unregulated supply could manifest in different frequencies, and therefore the PSRR specification must be stated with magnitude and frequency. For this specific design, a PSRR of at most -40 dB @ 10 kHz must be guaranteed.

Delivering a fast LDO is also important. The circuit must be able to respond to sudden changes in both the output current load, and the input voltage supply. The LDO must be able to respond to full load current changes of 1 μs, with an overshoot and undershoot no greater than 200 mV in the regulated output. Similarly, this circuit has to be able to withstand a 5 μs voltage shift of the input supply within the range of 2.0 and 2.5 V, with voltage peaks lower than 50 mV. The constraints on the overshoots and undershoots are established to avoid damages in the circuitry.

1.3 Methodology

A thorough research on fully integrated LDOs was conducted in order to gather information on the most recent techniques and results. Every topology proposal was analyzed in order to understand its contributions, as well as its shortcomings. This allowed for a specific combination of a few techniques that work well together and deliver a high performance LDO.

The study and modeling of the modifications done to the traditional LDO schematic were the starting point of the process. After the selection was completed, the design was initiated with the establishment of the high level structure specifications. This, in turn, led to initial simulations with some ideal internal sub-blocks in order to verify the performance of the entire system.

Once the high level structure was verified, the specifications for the internal sub-blocks, such as the error amplifier, were drawn. From those specifications, the design of all the circuits was performed.

Later on, several simulations were executed for validation purposes. Furthermore, a simulation that verify the performance of the circuit outside of the nominal conditions was necessary in order to assure the proper behavior of the system under a stress environment. Hence, a Monte Carlo analysis, which statistically emulates process variations as well as mismatch effects, was the final one to be conducted.

After the Monte Carlo analysis delivered positive results, the layout design of the circuit was the next step. Right after the layout design was realized, the same simulations run before were executed once again to the post-layout extracted circuit in order to validate the physical design. Finally, the layout design was sent to the foundry to be fabricated.

1.4 Structure of Work

This dissertation is organized in 5 chapters that illustrate the sequence of the design stages of the output-capacitorless LDO.

In **Chapter 2**, the highlights of the bibliographical revision are presented. The main published innovations and techniques concerning fully integrated LDOs are analyzed and described. The study of the principal past publications serves as background to the development of the LDO presented in this dissertation.

The entire schematic design of the LDO is described in **Chapter 3**. A description of the internal sub-circuits, such as the error amplifier, along with the detailing of both frequency stability improvement and slew rate enhancement additional blocks. First, an analytical study is conducted to get a better grasp on the behavior of the circuit. Then, from the drawn equations and curves, the actual transistor dimensioning is performed.

Following the established design flow, the layout design of the circuit is detailed in **Chapter 4**. Some mismatch reduction techniques are explained and illustrated in the layout of the LDO.

Several simulations are shown in **Chapter 5** in order to verify the performance of the circuit. Simulations with both nominal conditions and PVT variations were conducted.

Finally, **Chapter 6** comprises the conclusions drawn from the obtained results. The major findings of this design along with some proposals for future work are stated and discussed.

Chapter 2

Bibliographical Revision

The classical structure of an LDO with an external capacitor (C_L) is depicted in Figure 2.1. It basically consists of a passing element - usually a PMOS transistor - in charge of delivering the current demanded by the load (I_{LOAD}), and an error amplifier (EA), whose mission is to regulate the gate voltage of the passing element through a feedback loop in order to maintain the output voltage at the required value [1].

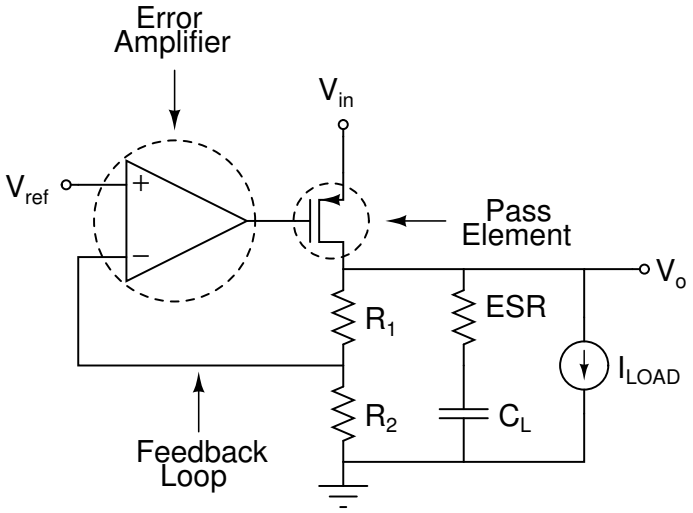


Figure 2.1: Schematic of classic LDO.

The dropout voltage of the LDO is the difference between the unregulated input voltage (V_{in}) and the regulated output (V_o). The lower the dropout voltage, the higher the power efficiency of the regulator. Moreover, the EA acts as a comparator and uses a reference voltage (V_{ref}) that is provided by a bandgap source (temperature variation resilient). One or two-stage operational amplifier (op-amp) are the common choices for the EA. The feedback loop is usually conformed by a resistor network that acts as a voltage divider in order to allow the comparison of V_o to V_{ref}. Finally, the external capacitor is modeled as a capacitance with an equivalent series

resistance (ESR). This element fulfills a double function: it sets the dominant pole and a left-hand-plane (LHP) zero, thereby improving the stability of the circuit. Moreover, its large capacitance value serves as a charge/discharge outlet for sudden load current changes and enhances the transient response of the circuit [1, 2].

In order to make the transition to fully integrated LDOs, several changes have been applied to the traditional structure described above. Modifications on the error amplifier, the addition of some extra block, or a mixture of both are the main explored options.

Regarding the variations in the error amplifier, the main innovations registered in the literature are the following:

- Class AB Structure
- Operational Transconductance Amplifier
- Flipped Voltage Follower

Concerning the changes in the overall structure of the LDO, the highlights of the literature are listed below:

- Active Feedback
- Adaptive Biasing
- Dynamic Biasing
- Resonance Factors Adjustment
- Hybrid Cascode

There are several other techniques registered in the literature - such as the ones described in [3–7] - that present remarkable innovations and results. However, they fall short to the fact that they all require an output capacitor to work properly, and thus are out of the scope of this dissertation.

2.1 Error Amplifier

2.1.1 Class AB Structure

The class AB amplifier contributes with several benefits compared to the classic two-stage and one-stage op-amps. First of all, this structure delivers a high-gain inverting amplifier, which comes in handy when using Miller compensation and other feedback techniques for frequency stability purposes. Additionally, the control

of the frequency poles becomes a much easier task due to the fact that the output stage of the amplifier is semi-isolated from its input stage. The latter is a key feature since the output stage of the amplifier will drive the power transistor of the LDO. Hence, the speed of the LDO will be constrained by the amount of current passing through its output stage and into/from the parasitic capacitance at the gate of the power transistor. On top of that, the equivalent impedance of the output stage along with the parasitic capacitance of the power transistor define one of the frequency poles of the circuit. Therefore, the trade-off between fast transient response and frequency stability has to be managed carefully. A generic type-N Class AB amplifier is depicted in Figure 2.2. The type-P equivalent of the circuit works too, and, depending of the operating voltage and reference voltage available, it is a suitable choice as well.

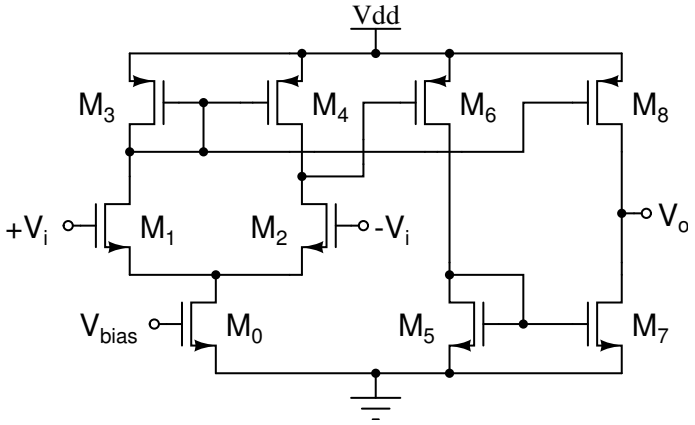


Figure 2.2: Schematic of type-N class AB amplifier.

As mentioned before, this amplifier achieves high open-loop gain (OLG) as well as signal inversion. Transistors M_0 through M_4 form the first stage (stage I) of the amplifier; while transistors M_5 through M_8 act as a non-inverting second stage (stage II). Nevertheless, the actual output stage - the one that sets the output impedance of the amplifier - is established by transistor M_7 and M_8. This means that the parasitic capacitance of these transistors - set by their aspect ratio - no longer have such a direct impact on the output capacitance of the first stage, as it is the case for a common two-stage op-amp; which ultimately translates to fewer constrains in the design process. Thus, the semi-isolation characteristic of the output stage mentioned above is explained. Additionally, transistors M_7 and M_8 behave as a push-pull stage that charges and discharges the gate capacitance of the power transistor of the LDO when fast transient variations take place. Additionally, a feedforward path is established by M_1, M_3 and M_8. This causes a zero on the right-hand side of the complex plane (RHP), generally located after the UGF so it does not affect the frequency stability [8, 9]. Both stages of the amplifier along with the

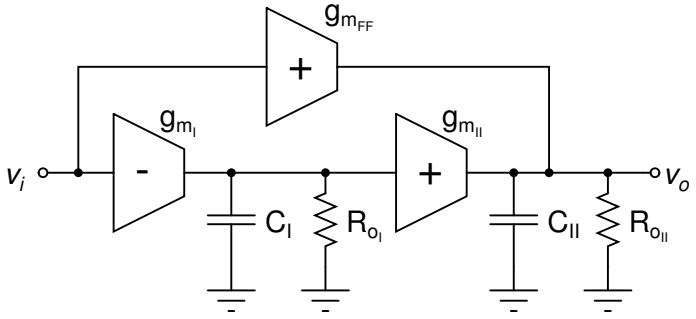


Figure 2.3: Small-signal model of class AB amplifier.

feedforward loop are better illustrated in Figure 2.3, where g_{m_i}, C_i and R_{o_i} refer to transconductance, output capacitance and output resistance of the i-th stage, respectively. The small-signal OLG of the class AB amplifier is defined as

$$A_{OLG}(s) \approx \frac{-g_{m_I} R_{o_I} g_{m_{II}} R_{o_{II}} (1 - s\frac{g_{m_{FF}} C_1}{g_{m_I} g_{m_{II}}})}{(1 + sR_{o_I} C_I)(1 + sR_{o_{II}} C_{II})}. \tag{2.1}$$

In terms of small-signal performance, the class AB amplifier is a very suitable choice. Nevertheless, the large-signal performance is a bit limited. In LDOs in general, the slew rate (SR) limiter is the gate capacitance of the power transistor, which is also the output capacitance of the EA. Therefore, the value of this capacitance and the amount of current passing through the amplifier's output stage determine the SR of the LDO. Since the output current of the class AB amplifier is a fixed multiple of its base current, it can be stated that the speed of the transient response is bounded to its fixed base current. The obvious solution would be to design a high current output stage, but this would compromise the frequency stability. Therefore, the trade-off between SR and frequency stability has to managed consciously. It is important to mention that the feedforward path within the amplifier aids the push-pull behavior of its output stage, and thus improves its transient response.

Versions of this amplifier - some with minor variations - have been widely used [8–11]. In [9] the first stage of the class AB amplifier is a folded cascode, which allows for even higher gain and high output impedance. Similarly, in [11] the output stage of the class AB amplifier is cascoded, thereby achieving higher gain and higher output impedance as well. The high output resistance eases the establishment of the dominant frequency pole. Though these benefits facilitate the LDO design, the cascode technique requires a minimum headroom voltage in order to maintain all transistors saturated. Thus, either the LDO is only suited for high unregulated input voltages [9], or the amount of output load current is limited in order to maintain the gate voltage of the power transistor within the appropriate range [11].

2.1.2 Operational Transconductance Amplifier

The use of an operational transconductance amplifier (OTA) as the error amplifier has its advantages. The main one is that the amount of current that drives the capacitance at the gate of the power transistor is no longer fixed, as it is in the case of an op-amp. For a differential OTA, the output current has a quadratic dependence to the input voltage, according to the square law of the MOS transistor [12–14]. However, the main drawback is that the achievable OLG and UGF are not as high as the ones obtained with an op-amp. Moreover, achieving frequency stability with no load present is quite difficult, to the extend that a minimum load current is always necessary [12–14]. Additionally, it is custom to employ a buffer amplifier between the reference voltage and the EA. Since the OTA does not present an infinite input impedance, the buffer is necessary to isolate the reference voltage from the rest of the circuit. Therefore, another disadvantage is the need for more circuitry. Nevertheless, the non-infinite input impedance of the OTA proves to be quite useful since it ends up in parallel with the output current load of the LDO in closed-loop configuration; this, in turn, helps with the frequency stability of the circuit [12–14]. The schematic of a simple OTA cell is depicted in Figure 2.4.

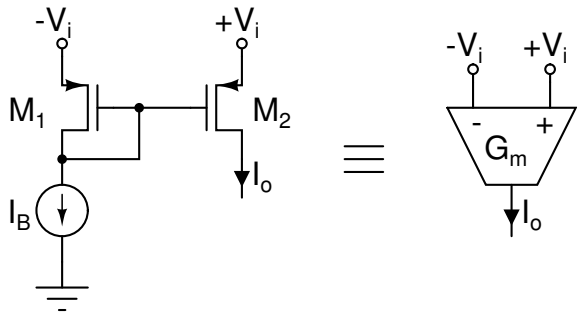


Figure 2.4: Schematic of differential OTA cell.

As it can be observed, the OTA cell consists of a base current (I_B) and a pair of matched transistors (M_1 and M_2) - which implies $g_{m_1} = g_{m_2} = G_m$ - in the form of a current mirror [12]. The ratio of the current mirror may change in order to scale the output voltage of the LDO to the available reference voltage. This suppresses the need of the feedback resistive network usually employed to link the LDO output voltage with the input reference voltage (Figure 2.1). Hence, the input impedance of the OTA affects directly the impedance at the output node of the LDO, as it was mentioned above. The OTA cell behaves as a differential common-gate error amplifier, which, even though somewhat solves the SR issue, presents a limited input common-mode range (ICMR). The minimum input voltage of the amplifier is set by the saturation voltage of the current source I_B and the source-gate voltage of M_1. As a consequence, this technique is not suitable when the output voltage is a low

value (low-voltage applications) [13, 14]. After performing a small-signal analysis of the OTA cell, the output current (I_o) can be expressed as:

$$I_o \simeq -G_m \Delta V_i. \tag{2.2}$$

Furthermore, the input resistance (R_i) of the OTA cell can be defined as:

$$R_i \approx \frac{1}{G_m}. \tag{2.3}$$

In order to make the OTA equally fast to both ascending and descending transient variations of the output voltage, a cross-coupled configuration of two OTA cells is necessary [12]. The circuit diagram is shown in Figure 2.5.

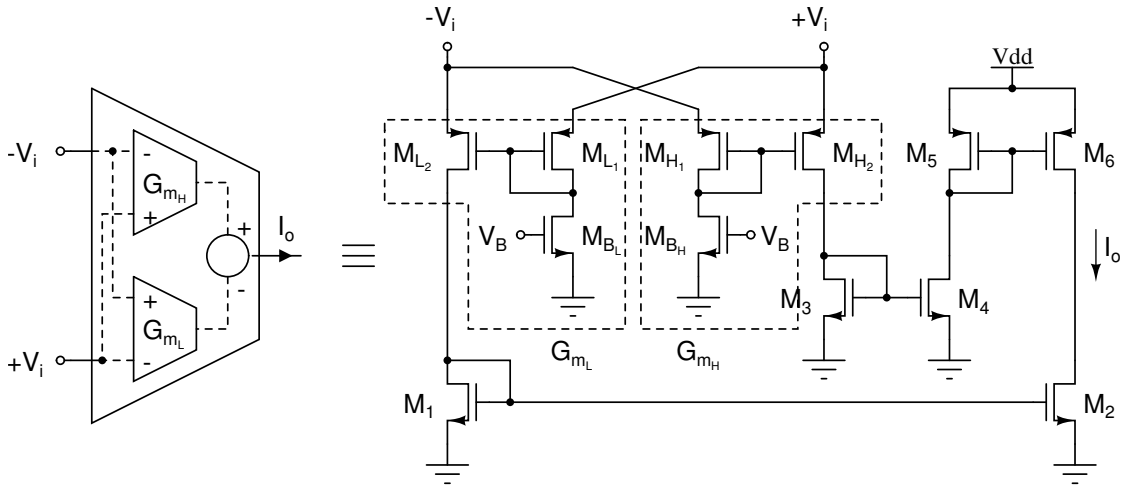


Figure 2.5: Schematic of cross-coupled OTA.

The cross-coupled OTA cells act as one single OTA that follows equations (2.2) and (2.3) as well. In [13, 14], small changes are made to the OTA structure detailed in [12]. In these articles, a double cross-coupled OTA configuration is used. This means that the structure is the same as the one in Figure 2.5, except that each internal OTA consists already of two cross-coupled OTA cells, whereas this might seem to imply the use of more circuitry, however, each cross-coupled OTA reuses the other one in order to optimize die area. Additionally, a current subtracter is placed to form a positive feedback loop within the OTA. The effect of this additional block is an overall transconductance increase, which finally translates to an OLG increase.

2.1.3 Flipped Voltage Follower

The flipped voltage follower (FVF) is a well known building block specially suited for low-power low-voltage analog applications. The reduced output impedance due to shunt feedback connection is the main feature of the FVF, and allows for good

regulation and frequency stability in LDO design [15]. Furthermore, the fact that the core of most FVFs is one single transistor establishing a direct path between the output and the input ensures a fast transient response. Moreover, the simplicity of the FVF structure helps to save die area. There is one main flaw nonetheless: the attainable OLG with the FVF is not as high as it is with other amplifiers [16]. Consequently, both load regulation and PSRR performances are degraded. The schematic of a simple LDO using a single-transistor FVF as the EA is depicted in Figure 2.6.

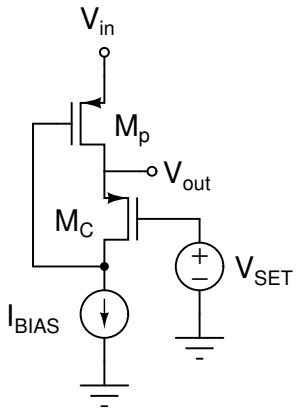


Figure 2.6: Schematic of single-transistor FVF-based LDO.

As it can be noticed, M_C (control transitor) behaves as a common-gate amplifier. Its source terminal acts as a sensor of the output voltage, so that when a variation occurs, M_C generates an error voltage at its drain terminal to control the gate voltage of M_P (power MOSFET). Thus, the amount of current drained by M_P is controlled and, in turn, the output voltage (V_{out}) is regulated [15]. The value of the preset voltage (V_{SET}) is determined by the following expression:

$$V_{SET} = V_{out} - V_{SG_C}, \tag{2.4}$$

where V_{SG_C} is the source-gate voltage of M_C. The fact that this transistor has a constant biasing (I_{BIAS}) makes it totally independent from the output current of the LDO. However, the expression in (2.4) indicates that V_{out} is highly sensitive to temperature and process variations, due to the strong dependency on V_{SG_C}. Consequently, V_{SET} must be provided by a specific circuit that tackles these issues [15]. A preset voltage generation circuit is shown in Figure 2.7. It consists basically of a simple unity-gain amplifier with the addition of transistor M_{C_3} set in diode connection and biased by I_{BIAS} (same bias level of M_C) at the output stage. A temperature-independent reference voltage (V_{REF}) - usually generated by a bandgap voltage reference - is placed at the input of the amplifier and regenerated at its output [15, 17]. Thus, V_{SET} is given by

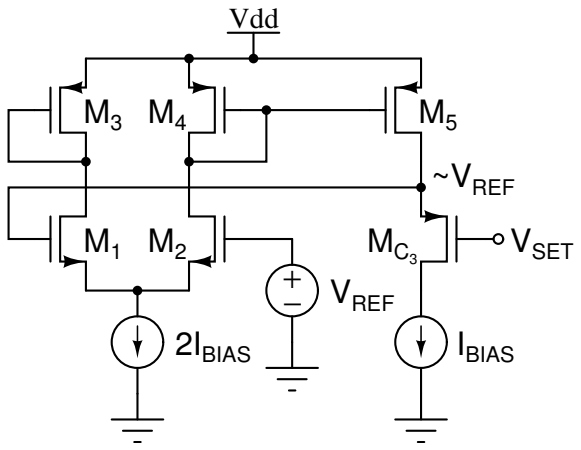


Figure 2.7: Schematic of preset voltage generator for FVF-based LDO.

$$V_{SET} = V_{REF} - V_{SG_{C_3}}, \tag{2.5}$$

where $V_{SG_{C_3}}$ is the source-gate voltage of M_{C_3}. Since M_{C_3} and M_C are matched transistors and have the same bias condition, their source-gate voltages are equal as well [15, 17]. Therefore, the relation stated below applies:

$$V_{out} = V_{REF}. \tag{2.6}$$

Thus, the regulation of the output voltage of the LDO is achieved. Another approach to implement an EA using the FVF is to use two control transistors instead of just one. This improves both OLG and SR without loosing the output impedance feature of the single-transistor FVF. The schematic of an LDO using a 2-transistor FVF as the EA is depicted in Figure 2.8.

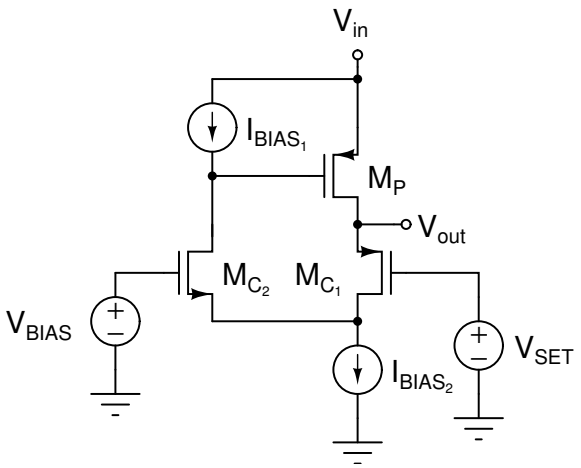


Figure 2.8: Schematic of 2-transistor FVF-based LDO.

As it can be observed, the structure is quite similar to the single-transistor FVF-

based LDO (Figure 2.6). There is one main control transistor (M_{C_1}), which means that equation (2.4) still applies (replacing V_{SG_C} by $V_{SG_{C_1}}$). Furthermore, the same preset voltage generating circuit (Figure 2.7) is used for the 2-transistor FVF. Hence, equation (2.6) is valid as well. The effect of the second control transistor (M_{C_2}) is manifested in the OLG of the amplifier (as one more gain stage), and in the transient response of the circuit. When the output current load rapidly increases, the LDO is not able to augment the source-gate voltage of M_P (V_{SG_P}) instantaneously to provide current due to its large gate parasitic capacitance, causing V_{out} to drop. As a consequence, $V_{SG_{C_1}}$ drops as well, to the point that MC_1 enters the cutt-off region momentarily, thus rendering I_{BIAS_1} - I_{BIAS_2} as the discharging current of the parasitic capacitance. Likewise, when the output current load suddenly decreases, the LDO cannot reduce V_{SG_P} immediately, which causes V_{out} to rise. This, in turn, causes the drain voltage of M_{C_1} to increase almost as high as V_{out}, due to the low resistance of the source terminal of M_{C_2}. Consequently, M_{C_2} enters the cut-off region momentarily, which renders I_{BIAS_1} as the charging current of the parasitic capacitance [17].

Many implementations of the FVF-based LDOs have been reported in the technical literature [15–18]. In [15, 18], a single-transistor FVF-based LDO - identical to the one depicted in Figure 2.6 - was presented. Regarding 2-transistor FVF-based LDOs, [16, 17] are the publications that standout the most. In [17], an LDO identical to the one portraited in Figure 2.8 was implemented. An SR enhancement block is added to further improve the transient response of the LDO. Moreover, in [16], a slight change is applied to the 2-transistor FVF structure. A non-inverting gain stage is added to boost the OLG of the LDO, and thus attaining higher PSRR, and better line and load regulations. Moreover, a very similar SR enhancement block to the one described in [17] is added as well. Both publications show good results in terms of transient response. Nevertheless, they both require a minimum load current to maintain stability.

2.2 LDO Structure

2.2.1 Active Feedback

In most LDOs, specially the ones featuring an op-amp as the EA, achieving frequency stability in all load conditions becomes a difficult task to undertake. Usually the op-amp posseses one dominant frequency pole and at least one secondary pole. Since the equivalent gate capacitance of the power transistor is already quite big, it is more feasible to design the op-amp so that its output stage sets the dominant pole of the entire LDO . The secondary pole of the LDO may switch between the

secondary pole of the op-amp and the pole generated by the output current load and the output capacitance. Because there is no external capacitor, the output capacitance is generated by the parasitic capacitance of the metal paths in charge of power distribution within the integrated circuit. If designed properly, the secondary pole of the op-amp will be located after the UGF of the LDO, and thereby will have no effect on the stability of the system. However, the frequency pole generated by the output current load is not fixed, and eventually falls behind the UGF as the current load decreases, thus causing instability. The worst case takes place when no current load is present [9, 19].

The approach of the active feedback technique is to modify and control both the dominant and the secondary frequency pole of the LDO, through a feedback path formed by a capacitor and a transconductor. Thus, the negative effect of the frequency pole generated by the output current load is neutralized. Usually a LHP zero is also generated by the active feedback technique, which could be used to further improve the frequency stability. Nevertheless, there is a downside to this technique: a set of complex poles are generated, which could degrade the stability of the system [9, 19].

The active feedback path has to be placed strategically within the LDO. The rule of thumb is the following: the input node of the path should be tied to the load that causes the problematic secondary pole, and the output node should be chosen to generate the dominant pole. The small-signal equivalent of a simple LDO, with a single pole op-amp as the EA, and the active feedback elements, can be visualized in Figure 2.9, where g_{m_1}, R_1 and C_1 are the transconductance, output resistance, and load capacitance of the EA, respectively. Moreover, g_{m_P} is the transconductance of the power MOSFET, R_o represents the current load of the LDO, C_o is the output capacitance caused by the power distribution rails, and C_{af} and g_{fa} are the capacitance and transconductor of the active feedback path, respectively. It is important to mention that C_1 consist mainly of the parasitic capacitance of the

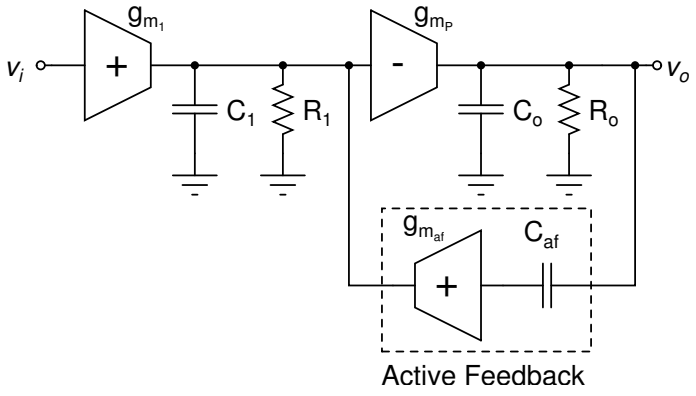


Figure 2.9: Small-signal model of simple LDO with active feedback.

power MOSFET. Assuming that $g_{m_{af}}$ has an input resistance R_{af}, then by standard circuit analysis methods, the transfer function is obtained as

$$A_{OLG}(s) = \frac{-g_{m_1} R_1 g_{m_P} R_o}{(1 + sR_1C_1)(1 + sR_oC_o) + sR_1[g_{m_P} R_o(g_{m_{af}} R_{af} C_{af})]}. \tag{2.7}$$

From (2.7) another benefit of the active feedback can be noticed: the quasi-Miller compensation using C_{af}. The capacitor is boosted by the gain of the power transistor stage ($g_{m_P} R_o$). However, the gain of the active feedback path ($g_{m_{af}} R_{af}$) arises solely from this specific configuration of its transconductor and the parallel input resistance. Furthermore, this compensation scheme is better than the traditional Miller because it boosts the capacitance and performs pole splitting, without generating the undesired RHP zero [19]. Assuming $R_1 g_{m_P} R_o g_{m_{af}} R_{af} C_{af} \gg R_1C_1 + R_oC_o$, the dominant pole ($\omega_{P_{dom}}$) and the secondary pole (ω_{P_2}) can be expressed as

$$\omega_{P_{dom}} \cong \frac{1}{R_1[g_{m_P} R_o(g_{m_{af}} R_{af} C_{af})]}, \tag{2.8}$$

$$\omega_{P_2} \cong \frac{g_{m_P}(g_{m_{af}} R_{af} C_{af})}{C_o C_1}. \tag{2.9}$$

From (2.9) it can be noticed that the secondary pole is no longer tied to the changing output current load, and therefore the frequency stability is ensured. However, this analysis is assuming an ideal transconductor in the active feedback path, which is never the case for real circuit implementation. The transconductor will cause the appearance of a set of complex poles and this will complicate the task of achieving stability.

LDOs using active feedback have been reported in [9, 19]. In [19], a very similar structure to the one depicted in Figure 2.9 was used to achieve stability and to improve the transient response of the circuit. The dominant pole is established at the gate of the power transistor with the active feedback path, which simultaneously provides a sensing device for the output voltage and a direct path for current charging/discharging of the gate capacitance of the power MOSFET. In [9], a slightly different approach was taken. The active feedback was used to set the dominant pole at the first stage of a class AB amplifier. This allowed for a higher gain due to the quasi-Miller compensation, which reduced the size of the active feedback capacitor. Furthermore, the transconductor design was less complex, making use of a common-gate topology instead of a common-source one (as in [19]). Both LDOs achieved frequency stability even when no load is present, while maintaining a low quiescent current. However, the LDO presented in [9] was able to withstand a higher maximum current load and achieved higher OLG and UGF.

2.2.2 Adaptive Biasing

A fast transient response is a highly demanded feature for LDOs. The LDO must be able to respond quickly to sudden variations of both the current load and the unregulated power line. In general terms, the former represents a tougher challenge than the latter, because when the current load changes, the operation region of the power transistor changes with it. When no current load is present at all, the power transistor is driving only the quiescent current, which is usually very small - commonly in the range between tens and hundreds of microamperes - in order to keep the power consumption low. Thus, the power transistor falls into the subthreshold region, where the relationship between its source-gate voltage and its drain current is exponential. For light loads, the power transistor will also remain in this region. When the current load reaches a medium level, the power transistor enters the saturation region, where the correlation between its source-gate voltage and its drain current is quadratic. In these two regions, the transient response of the LDO is considered quite fast, since a relatively big change in the load current translates to a small adjustment of the gate voltage of the power MOSFET. However, when dealing with heavy loads, the power transistor enters the linear region, and, consequently, the dependency of the drain current towards the source-gate voltage becomes linear as well. Therefore, an equal factor of increment in the drain current demands a larger increment of the gate-source voltage [13, 14, 20]. As a result, the LDO transient response becomes somewhat lethargic at the heavy-load condition, which manifests in the output voltage as large voltage spikes with high settling times. In order to achieve a faster response in the linear region, the LDO requires higher bandwidth and higher SR for charging/discharging the gate capacitance of the power MOSFET in response to the same factor of load change in the same period of time [13, 14, 20].

One logical solution to increase both bandwidth and SR is to augment the bias current of the EA. An increment in the bias current causes a shift in the frequency response of the amplifier, and thereby of the entire LDO. Recalling the relationship between the drain-source resistance (r_{DS}) and the drain current (I_D) of the MOS transistor

$$r_{DS} \; \alpha \; \frac{1}{I_D}, \tag{2.10}$$

it can be inferred that the higher the I_D gets, the lower the r_{DS} becomes. It is also important to remember that most pole frequencies (ω_p) in amplifiers are determined by the value of r_{DS}, since it becomes the output resistance of each stage, that is,

$$\omega_p = \frac{1}{r_{DS} C_p}, \tag{2.11}$$

where C_p stands for the parasitic capacitance at the output node. Thus, a reduction in r_{DS} translates to an increment in the pole frequency. As a consequent, an increment in the bias current of the amplifier pushes the poles forward in the frequency spectrum, thus attaining a higher bandwidth (higher UGF). Nevertheless, this usually causes a decrease in the OLG that could degrade the performance of the LDO. Furthermore, pushing the UGF to higher frequencies is also risky since it gets closer to other parasitic poles and zeros of the transfer function. Ultimately, this could reduce the phase margin (PM) and compromise the circuit stability.

Regarding the SR enhancement, it was stated before that the gate capacitance of the power MOSFET, which is also the output capacitance of the EA, is the main SR limiter of the LDO. So, recalling the definition of SR,

$$SR = \frac{I_o}{C_L}, \tag{2.12}$$

where I_o and C_L are the output stage current and the load capacitance of the amplifier, respectively, it is logical to infer that SR increases with the output current. Since the output current is a fixed multiple of the bias current of the amplifier, an increase in the latter will manifest as an increase in the former. It is important to highlight that the expression in (2.12) only applies for amplifiers with no internal compensation capacitor. Additionally, more bias current implies more quiescent current, which, in turn, means more power consumption. As it can be noticed, the trade-off between stability, SR and power consumption is very complex and probably the most critical one in output-capacitorless LDO design.

Higher bias current appears to be a feasible solution to the transient response issue. However, it is only necessary for heavy loads, and it would be inefficient - and at some level even damaging - to consume more current than necessary. Therefore, adaptive biasing is a far more efficient solution, which is to provide more bias current only when the load demands it. There is one important disadvantage to this technique nonetheless: once the sudden transient variation of the current load is over, the bias current remains at its maximum value. This might not degrade significantly the current efficiency since the load is driving a high current, but nevertheless it does imply more power consumption when it is no longer needed. The operating principles of this technique are shown in Figure 2.10.

The adaptive biasing circuit consists basically of a sensing circuit that keeps track of the output current load, and a current mirror that provides extra bias current to the amplifier when necessary. The sensing circuit generates a current proportional to that of the output load, but at a much lower scale in order to maintain a decent current efficiency. Thus, when dealing with light loads, the current sensed and fed back to the EA by the adaptive biasing circuit is practically negligible. The

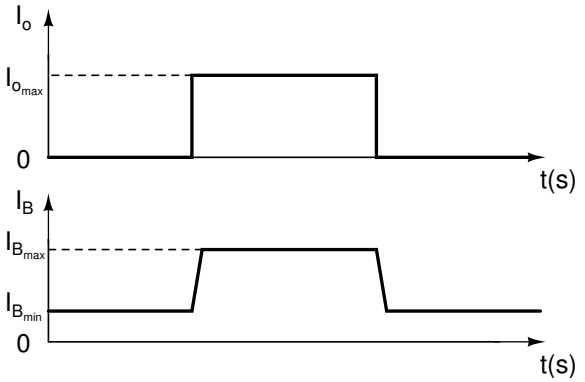


Figure 2.10: Adaptive biasing operating principles.

conceptual schematic of an LDO with adaptive biasing is depicted in Figure 2.11. The EA is assumed to be a type-N amplifier, but a type-P amplifier works as well. Moreover, if working with an OTA or FVF as the EA, the resistive feedback network is dispensable (as shown in sections 2.1.2 and 2.1.3).

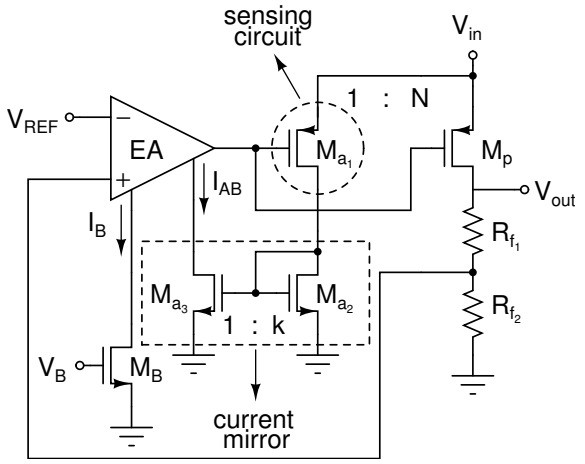


Figure 2.11: Conceptual Schematic of LDO with Adaptive Biasing.

The adaptive biasing circuit is implemented by transistors M_{a_1}, M_{a_2} and M_{a_3}. As detailed in the picture, M_{a_1} is the sensor of the adaptive biasing circuit. This transistor is biased by the same gate voltage as the power transistor (M_p), and hence, it will experience the same current changes as that of the load, but at a lower scale. The factor N determines the current proportion between the load and M_{a_1}. Therefore, since the current load reaches extremely high values, N should be large as well in order to keep the extra current at a minimum. Hence, the aspect ratios $(\frac{W}{L})$ of the aforementioned transistors are related by

$$\frac{(\frac{W}{L})_{a_1}}{(\frac{W}{L})_p} = \frac{I_{a_1}}{I_{out}} = \frac{1}{N}. \tag{2.13}$$

Transistors M_{a_2} and M_{a_3} form a current mirror that injects the extra current back into the amplifier. The factor k sets the gain of the current mirror and the relationship between the aspect ratios of the transistors, as N did for M_{a_1} and M_p. Ultimately, the maximum bias current ($I_{B_{max}}$) of the EA is

$$I_{B_{max}} = I_B + I_{AB}, \tag{2.14}$$

where I_B is the fixed bias current, and I_{AB} is the extra current generated by the adaptive biasing circuit.

Several implementations of LDOs using adaptive biasing have been published in the technical literature [13, 14, 20, 21]. In [20], a type-P counterpart of the circuit depicted in Figure 2.11 was used. In [13] and [14], the actual adaptive biasing circuit described in this section was utilized. The LDO presented in [21] employs an adaptive biasing technique implemented by an entire different circuit, following the same operating principle, nonetheless. A self-adaptive biased class AB OTA was featured in this implementation, which requires no current mirror, only a sensor to trigger the circuit. Additionally, a current amplifier aids even further the gain and transient response of the LDO. The LDOs presented in [13, 14, 20, 21] showed a fast response to load transient variations while consuming a very low quiescent current. However, they needed a minimum load current in order to maintain frequency stability. Additionally, the DC OLG at full-load condition was a bit low (under 60 dB). Moreover, the UGF goes down to the low hundreds of kilohertz range as the current load decreases. This means that, at medium and light load conditions, the noise components present in these "not so high" frequencies will couple more easily to the output voltage.

2.2.3 Dynamic Biasing

Another approach to address the SR issue while keeping the power consumption at a minimum and achieving stability is dynamic biasing. This technique is similar to adaptive biasing, except that it is far more efficient because, the quiescent current of the LDO is altered only during transient variations. Once the load current reaches a steady state, the quiescent current returns to its initial value, thereby reducing the average power consumption. Furthermore, since at the steady state the biasing of the LDO remains unchanged, the poles and zeros of the transfer function remain unaltered as well, thus ensuring stability. Hence, the bias current is modified to charge or discharge the gate capacitance of the power transistor, depending on whether the current load experiences a sudden decrease or increase, respectively. Since the EA drives the aforementioned gate capacitance, the technique is usually applied to its bias current or its output stage current directly [17, 22]. The operating principle of

the dynamic biasing technique is illustrated in Figure 2.12.

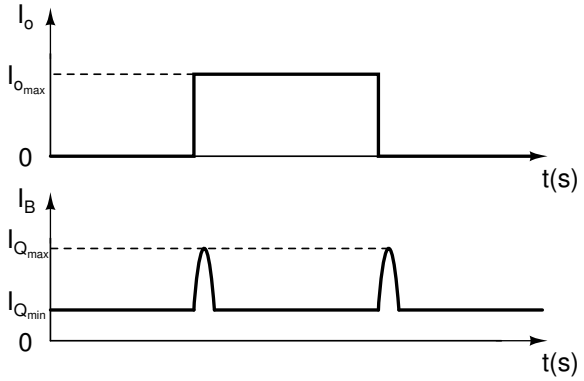


Figure 2.12: Dynamic biasing operating principal.

Similarly to the adaptive biasing technique, a sensing stage and a trigger stage are necessary in order to perform the dynamic biasing. Either an internal node of the LDO, or the actual output voltage could be the one that triggers the temporary quiescent current surge. However, it has been proven that in most cases monitoring an internal node works a bit faster than the output node, due to the longer signal path [22]. Watching the output voltage is a far less complex approach and makes the design process easier, nonetheless. In any case, the main tool to monitor sudden voltage changes is voltage spike detection through capacitive coupling. It basically consist of a simple current mirror linked to a passive network, as can be visualized in Figure 2.13.

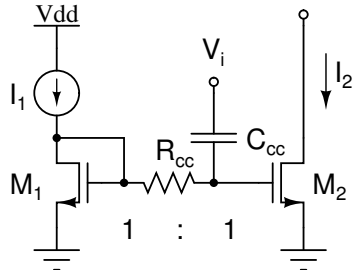


Figure 2.13: Schematic of voltage spike detection circuit through capacitive coupling.

The passive network consist of a basic RC (resistance-capacitance) circuit acting as a high-pass filter. Thus, any sudden variations (high frequency components) in the input voltage (V_i) will be detected and coupled to the gate of transistor M_2. On the contrary, when V_i is at its steady state, capacitor C_{cc} acts as an open circuit, thereby isolating the gate of transistor M_2 from V_i and shutting down the dynamic biasing feature. So, sudden voltage spikes in V_i are transfered to the gate voltage of M_2 (V_{G_2}), thus momentarily increasing the output current I_2. On the other hand, if V_i is constant, then the current mirror - with a current gain factor of 1 - behaves

normally, thereby yielding $I_1 = I_2$ [17]. The behavior of the voltage spike detection circuit through capacitive coupling can be better appreciated in Figure 2.14.

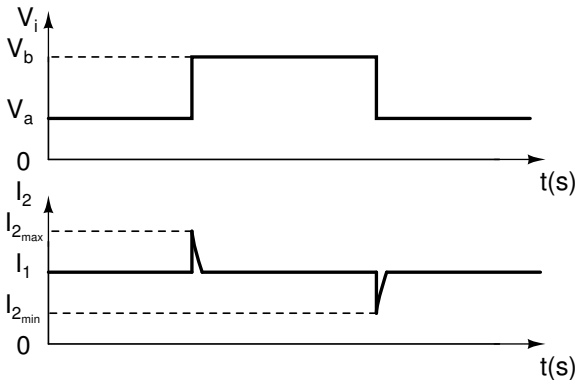


Figure 2.14: Behavior of voltage spike detection circuit through capacitive coupling.

As it can be observed, the output current (I_2) experiences rising and falling spikes due to the rising and falling voltage transitions of V_i, respectively. However, when V_i stabilizes, I_2 returns to its steady state value I_1. In order for this technique to work, C_{cc} has to be greater than the gate-source capacitances of M_1 and M_2, so that when transient variations occur, the gate voltage of M_2 is dominated by the voltage coupled through C_{cc} in that particular instant. Additionally, R_{cc} should be large in order to properly isolate M_1 and M_2 [14, 17, 22].

The actual momentarily injected - or extracted - current (ΔI_2) due to the sudden variation in V_i (ΔV_i) can be obtained from equation

$$I_2 + \Delta I_2 = \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_2(V_{GS_2} + \Delta V_i - V_{TH})^2$$

$$I_2 + \Delta I_2 = \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_2[(V_{GS_2} - V_{TH})^2 + \Delta V_i^2 + 2\Delta V_i(V_{GS_2} - V_{TH})], \qquad (2.15)$$

from which it follows that

$$\Delta I_2 \approx \frac{\mu_n C_{OX}}{2}(\frac{W}{L})_2(V_{GS_2} + \frac{\Delta V_i}{2} - V_{TH})\Delta V_i. \qquad (2.16)$$

From (2.16) it can be noticed that the larger the aspect ratio of M_2 ($(\frac{W}{L})_2$), the more current will be injected during the transient variation but at the penalty of consuming more quiescent current at the steady state [14, 17].

As mentioned above, the common strategy is to monitor the output voltage of the LDO ($V_i = V_{out}$). The reason for this is that the output voltage experiences rising and falling voltage spikes depending on the variation of the load current, thus providing a trigger signal to activate the dynamic biasing circuit. When the load current suddenly increases, the output voltage drops temporarily due to the fact that LDO is not able to discharge the gate capacitance of the power transistor so

quickly. On the other hand, when the load current suddenly decreases, the output voltage rises momentarily due to the fact that the LDO is not able to charge the gate capacitance of the power transistor in such a short period of time [14, 16, 17]. The behavior of the load current (I_o) and output voltage (V_{out}) is portraited in Figure 2.15.

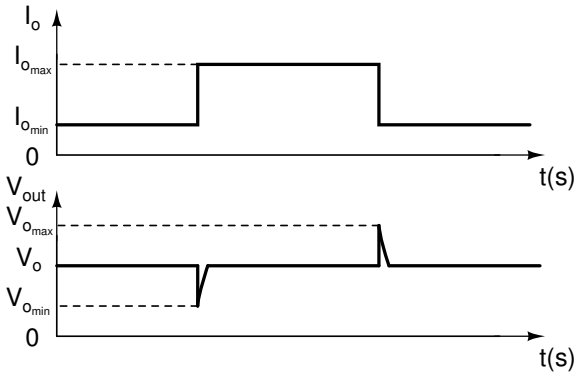


Figure 2.15: Transient behavior of load current and output voltage of an LDO.

The main objective of dynamic biasing is to minimize the overshoot and undershoot of V_{out}, so that the LDO delivers an acceptable supply voltage. Moreover, the settling time of these voltage transient variations are also reduced with this technique. Regarding the small-signal behavior of the dynamic biasing circuit, there is one important thing to mention: the RC network produces a LHP zero in the transfer function ($\frac{1}{R_{cc}C_{cc}}$). The location of this zero within the frequency spectrum has to be chosen carefully. The rule of thumb is to place it around the UGF of the LDO so that it increases the PM and, in turn, aids the frequency stability of the loop.

Many LDOs featuring dynamic biasing have been reported in the literature [9, 13, 14, 16, 17, 22]. In [16, 17] a voltage spike detection circuit as the one described in this section was implemented, which was connected to the output stage of the FVF chosen as the EA. However, the one reported in [16] proved to be more efficient since it only used one voltage spike detection circuit, whereas the one in [17] used two (larger die area). In [14], the same approach was taken, only this time to an OTA featured as the EA. Nevertheless, in [13] an extra SR enhancement block based on dynamic biasing was featured. This SR enhancement block acts as another push-push stage in parallel to the EA, driving the gate capacitance of the power transistor. The extra path is deactivated during steady state, as the dynamic biasing operating principle dictates. The LDO presented in [9] showed a slightly different approach: the voltage spike detection circuit used a transistor as a resistor, instead of the passive element. Furthermore, the voltage spike detection circuit has no steady state operation. It only works during transient variations, thereby reducing even

more the average quiescent current. All the LDOs mentioned so far monitor its output voltage, unlike the LDO presented in [22], where the bias voltage of the EA was the watched node in order to obtain a faster response. This LDO featured a slewing-detecting circuit that takes the bias voltage and generates trigger signals to activate the dynamic biasing. It is important to highlight that this LDO was the only one that did not require a minimum load current in order to maintain frequency stability.

2.2.4 Resonance Factors Adjustment

Several frequency stability improvement techniques have been revised so far. However, regardless of the chosen technique, the ultimate outcome always comprises one dominant pole (p_{dom}) and a set of complex poles ($B(s) = 1 + as + bs^2$), which can be described mathematically as

$$OLG(s) = \frac{A_o(1 + \frac{s}{z_1})}{(1 + \frac{s}{p_{dom}})(1 + as + bs^2)}. \tag{2.17}$$

In this scenario, it would seem that the only concern is choosing a proper location of the complex poles. Nevertheless, the issue is a bit more complex than just the frequency location, since complex pole peaking may appear in the frequency response, thus jeopardizing stability of the system. This phenomenon becomes more critical for light loads, as it can be observed in Figure 2.16.

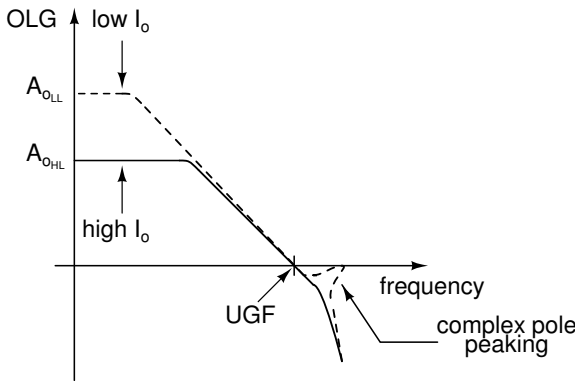


Figure 2.16: Frequency response of an LDO for different loads.

Any second-order frequency domain (S plane) expression can be analyzed as if it were a resonator. Thus, it can be modeled with the same parameters: natural resonating frequency (ω_o), quality factor (Q) and damping factor (ζ), as shown in the expressions below:

$$B(s) = 1 + (\frac{1}{Q\omega_o})s + (\frac{1}{\omega_o^2})s^2, \tag{2.18}$$

where

$$Q = \frac{1}{2\zeta}. \tag{2.19}$$

As a result, the complex pole peaking can be managed by controlling Q or ζ. Like any second-order system, it can be characterized as under-damped ($Q > \frac{1}{2}$), over-damped ($Q < \frac{1}{2}$), or critically damped ($Q = \frac{1}{2}$).

For the transfer function given in (2.17), the PM for light loads can be found as

$$PM = 90^\circ - \tan^{-1}\{\frac{\frac{UGF}{\omega_o}}{Q[1-(\frac{UGF}{\omega_o})^2]}\} + \tan^{-1}(\frac{UGF}{z_1}), \tag{2.20}$$

from which it can be noticed that a high ω_o increases the PM. Furthermore, the expression also indicates that with a high Q, the negative shift is reduced and a higher PM is attained. However, a high Q results in complex pole peaking, which could ultimately compromise the stability [8, 20]. Hence, a trade-off between a flat response and stability, while achieving a high UGF is established. In general terms, the optimum response for the LDO is the maximally flat one (no complex pole peaking whatsoever). Therefore, the ideal response is the one that resembles that of a Butterworth filter ($Q = \frac{1}{\sqrt{2}}$) [9, 10].

Techniques such as regular Miller compensation or active feedback generate an equation with one dominant pole and a set of complex poles, like the one detailed in (2.17). These techniques manage to generate non-dominant complex poles that are not directly correlated to the output load. Therefore, all that is left to do is to add a path within the LDO that allows to control Q and ω_o. The main purpose is to obtain the complex pole expression in terms of design parameters, such as transconductances and capacitances. One simple and effective way to accomplish this objective is to place one more capacitor in the EA and generate a second path between the output of its first stage and the the output of its second stage. This technique is called Q-reduction. An LDO featuring a class AB op-amp as the EA, Miller compensation, and a Q-reduction circuit is depicted in Figure 2.17. As it can be observed, the principal addition to the circuit is one single capacitor (C_Q). The other elements of the circuit are well-known: transistors M_0 through M_8 form the class AB EA, M_P is the power transistor, C_M is the Miller capacitor, R_{f_1} and R_{f_2} conform the resistive feedback network, C_{out} is the parasitic output capacitance due to the distribution rails, and I_L is the output current load.

It is worth mentioning that M_3 and M_4 act not only as the active load of the first stage of the amplifier, but also as a current buffer connected to the input of the second stage, creating a feedback path through C_Q and a feedforward path through M_8. The small-signal equivalent circuit of the LDO is depicted in Figure 2.18, where

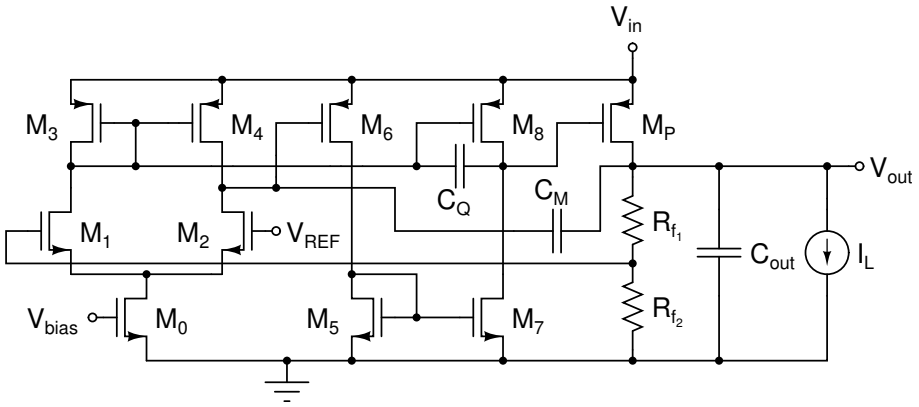


Figure 2.17: Schematic of LDO with Q-reduction technique.

$g_{m_{cb}}$, R_{cb} and C_{cb} are transconductance, input resistance, and input capacitance of the current buffer, respectively. Moreover, $g_{m_{FF}}$ represents the transconductance of the feedforward path. The rest of the elements follow the same notation used in Subsection 2.1.1 for the EA, and in Subsection 2.2.1 for the power transistor.

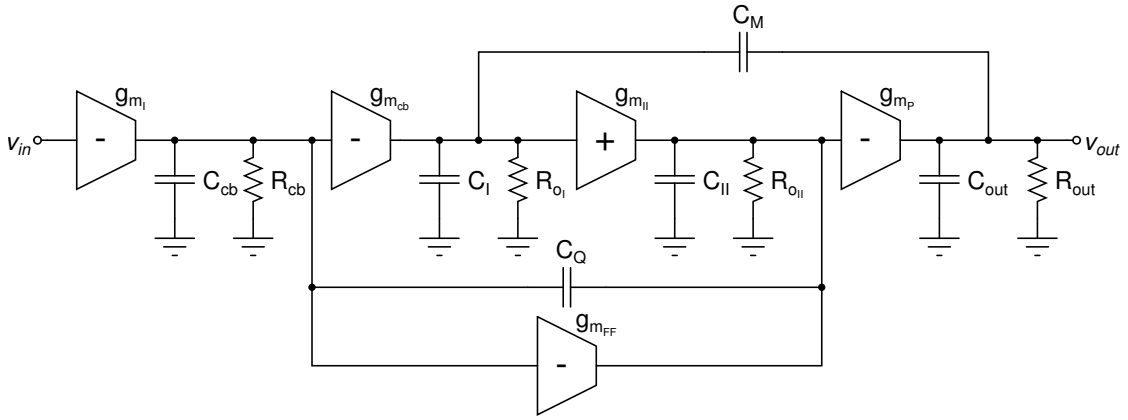


Figure 2.18: Small-signal equivalent circuit of LDO with Q-reduction technique.

The complex denominator polynomial ($B(s)$) of the circuit is aproximated by

$$B(s) \approx 1 + (\frac{C_Q}{g_{m_{cb}}} + \frac{C_Q C_{out}}{g_{m_P} C_M})s + (\frac{C_{out} C_2}{g_{m_{FF}} g_{m_P}} + \frac{C_Q C_{out}}{g_{m_{cb}} g_{m_P}})s^2. \tag{2.21}$$

From (2.21) and (2.18), results

$$\omega_o = \frac{1}{\sqrt{\frac{C_{out} C_2}{g_{m_{FF}} g_{m_P}} + \frac{C_Q C_{out}}{g_{m_{cb}} g_{m_P}}}} \tag{2.22}$$

and

$$Q = \frac{\sqrt{\frac{C_{out} C_2}{g_{m_{FF}} g_{m_P}} + \frac{C_Q C_{out}}{g_{m_{cb}} g_{m_P}}}}{\frac{C_Q}{g_{m_{cb}}} + \frac{C_Q C_{out}}{g_{m_P} C_M}}. \tag{2.23}$$

From (2.22) and (2.23) it can be observed that C_Q affects both ω_o and Q. The latter, nonetheless, has a stronger dependency than the former due to the fact that it presents a linear correlation, whereas the former presents a square root correlation to the capacitor. Thus, an increase in C_Q will reduce Q significantly, while slightly reducing ω_o. Hence, the trade-off between the location of the poles and a flat response has been revised.

The LDOs presented in [8, 10, 20] featured extra circuitry to control either Q or ζ. In [8, 20], the same Q-reduction technique studied here was utilized. However, in [10], a damping-factor-control circuit was used. In this paper, no extra feedback or feedforward path is established between the 2 stages of the EA. The added circuitry is a cross-coupled OTA with a capacitor linking its input to its output. This OTA is placed in parallel to the second stage of the EA, but with its output as a floating node. Though the circuitry is a bit different, the design criteria was also to attain $\zeta = \frac{1}{\sqrt{2}}$. The main downside to these techniques is that the UGF achieved is usually low (under 1 MHz), and a minimum load current is always necessary to maintain frequency stability. The LDOs featured in [9, 11] focused on other techniques to achieve frequency stability. Nevertheless, an analysis on Q or ζ of the non-dominant complex poles was conducted in order to attain a flat and smooth frequency response.

2.2.5 Hybrid Cascode

Another recent published technique that improves both stability and SR is hybrid cascode compensation. This technique is very similar to classic Miller compensation, except that it uses two capacitors instead of one. The end result is a better control of the non-dominant complex poles of the LDO, thus making the system stable while achieving high UGF [11].

An LDO featuring a single-stage amplifier with a cascoded active load as the EA is illustrated in Figure 2.19. Transistors M_0 through M_8 conform the EA, M_P is the power transistor, C_C is the cascode capacitance causing a Miller efect, R_{f_1} and R_{f_2} conform the resistive feedback network, C_{out} represents the output capacitance generated by the parasitic capacitances of the metal paths, and I_L represents the output current load. After drawing the small-signal equivalent circuit, the transfer function of the LDO can be expressed as

$$OLG(s) \approx \frac{A_o(1+\frac{s^2}{z^2})}{(1+\frac{s}{p_{dom}})(1+(\frac{2\zeta}{\omega_o})s+(\frac{1}{\omega_o^2})s^2)}, \tag{2.24}$$

where

$$A_o = (\frac{R_{f_2}}{R_{f_1}+R_{f_2}})g_{m_1}g_{m_P}R_1[r_{DS_P}||(R_{f_1}+R_{f_2})], \tag{2.25}$$

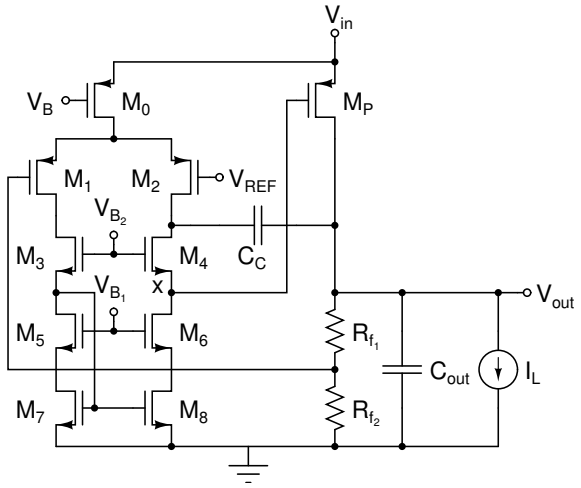


Figure 2.19: Schematic of LDO with classic cascode compensation.

$$z = \sqrt{\frac{g_{m_4} g_{m_P}}{C_x C_C}}, \tag{2.26}$$

$$p_{dom} = \frac{1}{R_x(C_x + g_{m_P}[r_{DS_P}||(R_{f_1} + R_{f_2})]C_C)}, \tag{2.27}$$

$$\omega_{o_c} = \sqrt{\frac{g_{m_4} g_{m_P}}{C_x(C_C + C_{out})}}, \tag{2.28}$$

$$\zeta_c = \frac{\frac{g_{m_4}}{2C_C}}{\sqrt{\frac{g_{m_4} g_{m_P}}{C_x(C_C + C_{out})}}}. \tag{2.29}$$

In the above equations, g_{m_i} and r_{DS_i} represent the transconductance and drain-source resistance of transistor M_i. Moreover, R_x and C_x represent the output resistance and capacitance at the node x.

The same LDO utilizing hybrid-cascode compensation is depicted in Figure 2.20. As it can be visualized, two compensation capacitors are used: C_{C_1} and C_{C_2}. This means that there are two feedback paths from the output voltage (V_{out}) to the node x. Regarding the large-signal response, each feedback path possesses its own time constant: $\tau_1 = \frac{g_{m_4}}{C_{C_1}}$ and $\tau_2 = \frac{g_{m_6}}{C_{C_2}}$. Logically, the optimal transient response of the LDO will be obtained when the two time constants are equal. In this scenario, equations (2.24) through (2.29) apply to this circuit as well, with two minor modifications: g_{m_4} is replaced by $(g_{m_4} + g_{m_6})$, and C_C by $(C_{C_1} + C_{C_2})$ [11].

Assuming $g_{m_4} = g_{m_6}$, and recalling expression (2.29), the damping factor of the non-dominant complex poles when using the hybrid cascode technique (ζ_{hc}) can be expressed as

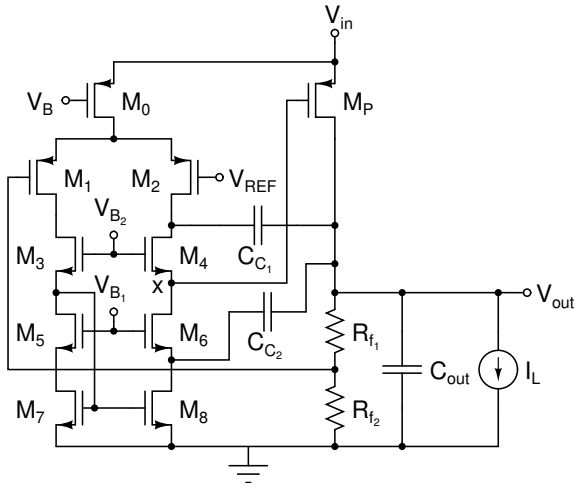


Figure 2.20: Schematic of LDO with hybrid cascode compensation.

$$\zeta_{hc} = \frac{\frac{(g_{m_4}+g_{m_6})}{2C_C}}{\sqrt{\frac{g_{m_4}g_{m_P}}{C_x(C_C+C_{out})}}} = \frac{\frac{g_{m_4}}{C_C}}{\sqrt{\frac{g_{m_4}g_{m_P}}{C_x(C_C+C_{out})}}} = 2\zeta_c. \tag{2.30}$$

Similarly, recalling (2.28), the frequency of the non-dominant complex poles when using hybrid cascode compensation ($\omega_{o_{hc}}$) is

$$\omega_{o_{hc}} = \sqrt{\frac{(g_{m_4}+g_{m_6})g_{m_P}}{C_x(C_C+C_{out})}} = \sqrt{2}\omega_{o_c}. \tag{2.31}$$

From (2.30) it can be deduced that the hybrid cascode technique attains a much flatter and smoother frequency response than does the classic cascode, using the same resources (die area, power consumption). Likewise, from (2.31) it can be noticed that hybrid cascode compensation allocates the non-dominant complex poles at higher frequencies than those of the classic cascode compensation. As mentioned above, another benefit of this technique is that it presents a balanced transient response. The premise that states the time constants are equal ($\tau_1 = \tau_2$) forces the circuit to respond equally fast to both sudden increase and decrease of the load current [11]. There is one downside to this approach: cascode technique always represents a challenge to low-voltage applications due to the minimum headroom required to maintain all transistors in the saturation region.

The hybrid cascode technique was presented in [11]. The LDO in this article achieved both high OLG and high UGF. However, the maximum current load supported was somewhat small due to the headroom limitation of the hybrid cascode technique. Moreover, the quiescent current of the circuit was a bit high. The LDO proved to be stable for all load conditions.

Chapter 3

Schematic Design

From all the techniques and topologies studied in Chapter 2, only three were chosen to implement the LDO. The final selection comprised active feedback, dynamic biasing, and a class AB op-amp as the EA. Furthermore, some innovations were implemented, such as the adaptive (load-dependent) and temperature resilient active feedback compensation scheme. Throughout this chapter a more thorough analysis of the LDO architecture will be presented. First, the proposed LDO structure will be introduced. Then, a closer look at the behavior of the circuit in both frequency and time domain will be taken. Next, the circuit implementation - including full transistor dimensioning - along with some design criteria will be described. Finally, the results of several simulations will be shown in order to verify the performance of the LDO schematic design.

3.1 LDO Structure

Figure 3.1 illustrates the structure of the proposed LDO. The main classic elements can be visualized: the power transistor (M_P), the EA, the resistive feedback network (R_{f_1} and R_{f_2}), the output capacitance generated by the power distribution metal paths (C_{out}), and the output current load (I_{LOAD}). The additional blocks can be easily noticed as well: the Miller compensation capacitor (C_m), the adaptive active feedback path (C_a, G_{m_a} and G_{m_b}), the dynamic biasing feedback path (C_{cc} and G_{m_f}), and the slew rate enhancement (SRE) path (C_{cc} and G_{m_x}). A high-speed loop is generated by G_{m_a} and G_{m_f}. These two paths implement a fast push-pull network that charges and discharges the gate capacitance of M_P. Additionally, another high-speed loop is established by G_{m_x}, which is only activated during transient variations and thereby has no effect on the steady-state response of the circuit. Hence, the LDO response time is reduced even more while keeping the average power consumption at a minimum. Moreover, due to its null steady-state operation, accuracy is not a requirement for this high-speed loop. The steady line and load regulation are

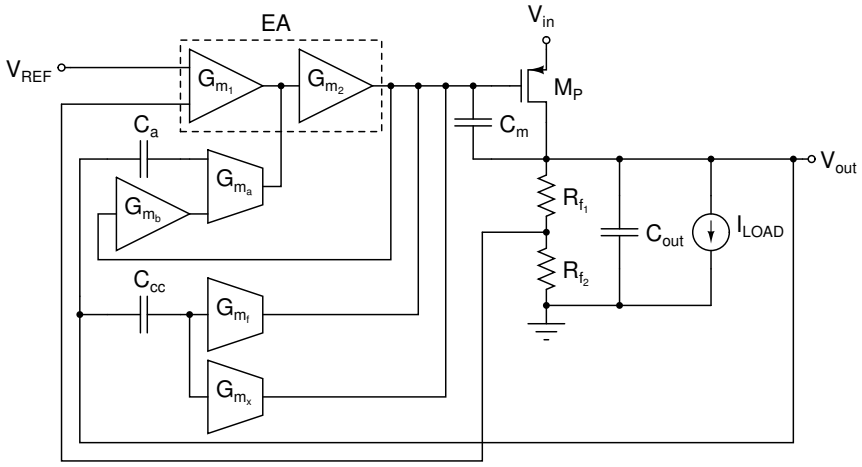


Figure 3.1: Conceptual Schematic of the proposed LDO.

determined by the high-gain loop.

The active feedback and the dynamic biasing feedback paths guarantee the stability of the loop. C_a and G_{m_a} along with C_{cc} and G_{m_f} cause the appearance of LHP poles and zeros in the transfer function that, if placed properly within the frequency spectrum, will cancel each other out and improve the PM without compromising the UGF. The active adaptive feedback plays a key role in this matter, since the location of the poles and zeros change according to the current load. However, as stated before, this elements influence not only the frequency response, but also the transient response. Thus, both the high-speed and the high-gain loop regulate the output voltage simultaneously, which might cause a set of non-dominant complex poles or non-split real poles and degrade the stability of the LDO, specially when driving a small load current. The idea is to push the non-dominant poles beyond the UGF and, when dealing with complex poles, maintain their Q equal to $\frac{1}{\sqrt{2}}$ for a maximally flat response. Therefore, the trade-off between SR and stability has to be managed carefully.

3.2 Small Signal Analysis

The open-loop small signal model of the proposed LDO is depicted in Figure 3.2. All the elements listed in the previous section can be visualized: first and second stages of the EA, the power transistor, the adaptive active feedback block, the dynamic biasing feedback block, and the SRE block. The dc gain of the LDO is given by the product of the gain of the EA and the power transistor. The first pole of the system is generated by the adaptive active feedback compensation capacitor C_a. However, as stated before, this capacitor generates a zero as well, which falls around the location of the pole thereby canceling each other out. The second pole

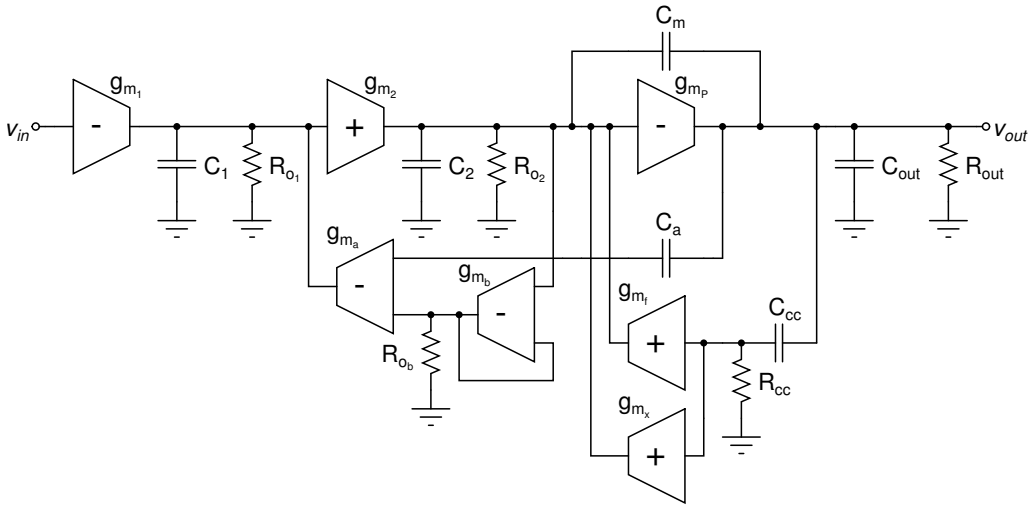


Figure 3.2: Small signal model of the proposed LDO.

of the system is generated essentially by the Miller compensation capacitance C_m and the output resistance of the second stage of the EA (R_{o_2}). Nevertheless, the adaptive active feedback compensation capacitance and transconductance - C_a and g_{m_a}, respectively - affect the second pole of the system as well. This pole becomes the dominant one. Furthermore, the third and fourth pole are also set mainly by the active feedback (C_a and g_{m_a}) and the second stage of the EA (C_m and R_{o_2}). Although, as the current load decreases, its impact on this poles increases, which could compromise the stability. In this scenario, the zero generated by the dynamic biasing capacitance (C_{cc}) nulls the effect of the third pole and restores the stability. As it can be noticed, the adaptive active feedback compensation elements affect all poles location.

In order to derive the actual open-loop transfer function ($A_v(s) = \frac{v_{out}}{v_{in}}$) the following asumptions have been made:

- Input resistance R_a of the adaptive active feedback block is equal to the inverse of its transconductance g_{m_a}.
- The compensation capacitors C_a, C_m and C_{cc} are much larger than the parasitic capacitances C_1 and C_2.
- The gain of each stage of the EA is much larger than 1.
- The SRE path (g_{m_x}) can be viewed as inactive since it only functions when output transient variations occur.
- Every transconductor in the small signal model is characterized as a common-source amplifier, with the exception of the active feedback one (g_{m_a}), which

presents a common-gate topology. Thus, it will be the only one drawing an input current.

In order to simplify the calculation process, it is best to understand the adaptive bias voltage generator (g_{m_b}) of the adaptive active feedback block by itself, so it can be later replaced by a less complex plain active feedback block that behaves as a common-gate amplifier with an arbitrary g_{m_a} value. This will facilitate the small-signal analysis of the LDO. The small signal model of the adaptive bias voltage generator is shown in Figure 3.3, where v_g represents the gate voltage of the power MOSFET (M_P), which is also the output voltage of the second stage of the EA, and v_{b_a} is the bias voltage at the gate of the active feedback transconductor (g_{m_a}).

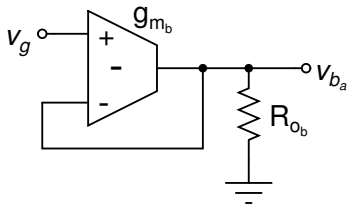


Figure 3.3: Small signal model of the adaptive bias voltage generator.

As it can be observed, the adaptive bias voltage generator is a common voltage follower. Its adaptive feature arises from the fact that it is driven by v_g. The dc operating point of M_P changes according to the current load variations, and so does its dc gate voltage. The expression for v_{b_a} is given by

$$v_{b_a} = \frac{g_{m_b} R_b}{1 + g_{m_b} R_b} v_g. \tag{3.1}$$

Assuming $g_{m_b} R_b \gg 1$, it renders

$$v_{b_a} \approx v_g. \tag{3.2}$$

So, as (3.2) shows, the circuit is a basic voltage follower. Therefore, v_g influences the current generated by the adaptive active feedback block. Figure 3.4 illustrates the active feedback transconductor (g_{m_a}), where v_{out} is the LDO output voltage and i_a is the current provided by g_{m_a}.

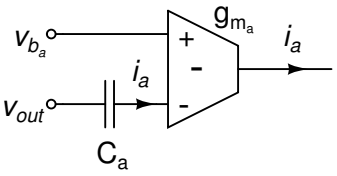


Figure 3.4: Small signal model of the adaptive active feedback block.

Hence, recalling (3.2), the expression for i_a is given by

$$i_a = -(\frac{sC_a}{1 + s\frac{C_a}{g_{m_a}}})(v_g - v_{out}) = (\frac{sC_a}{1 + sC_aR_a})(v_{out} - v_g). \tag{3.3}$$

If the small signal analysis of the circuit is further pursued using (3.3), the end result is an extremely complex transfer function [8, 20]. Additionally, it could be verified by simulation that the variations introduced by the v_g component appear in the location of the non-dominant poles and zeros, and are quite irrelevant. Therefore, the adaptive component (v_g) can be neglected in the small signal analysis, and the block can be perceived as a plain active feedback path with a variable transconductance (g_{m_a}). The transconductance variation is correlated to the load current shift: when the load current decreases, the dc gate voltage of M_P (V_G) increases, which in turn causes an increment of g_{m_a}, and viceversa. The resulting active feedback block with variable transconductance is depicted in Figure 3.5.

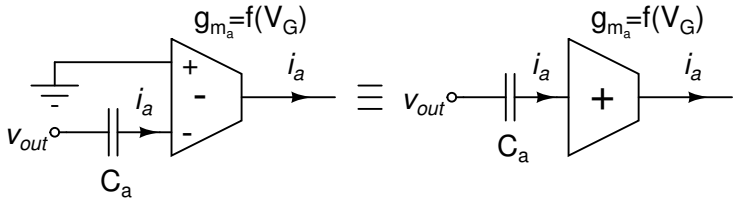


Figure 3.5: Simplified small signal model of the adaptive active feedback block.

Equation (3.3) is therefore reduced to

$$i_a = (\frac{sC_a}{1 + s\frac{C_a}{g_{m_a}}})v_{out} = (\frac{sC_a}{1 + sC_aR_a})v_{out}, \tag{3.4}$$

where $g_{m_a} = \frac{1}{R_a} = f(V_G)$. The new LDO small signal model is shown in Figure 3.6.

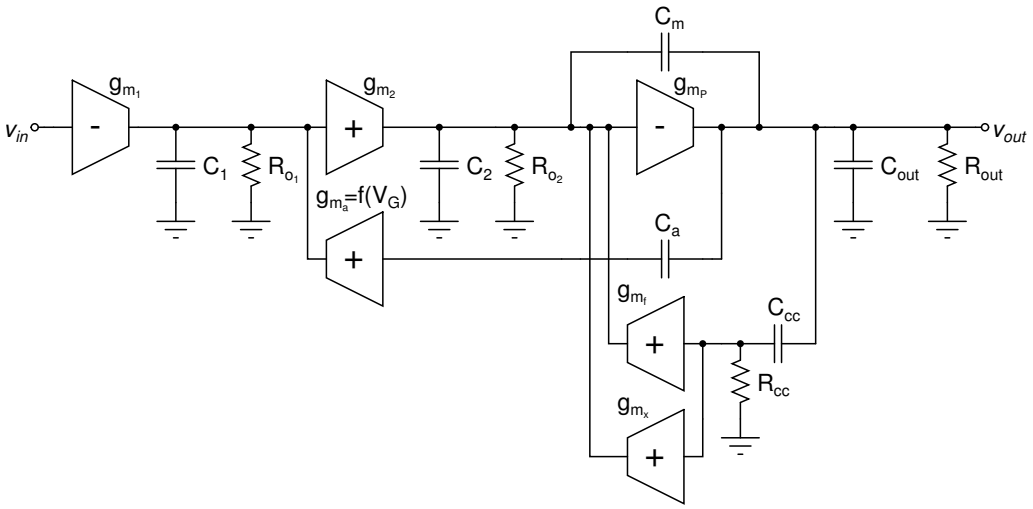


Figure 3.6: Simplified small signal model of the proposed LDO.

The simplified model of the LDO renders the following transfer function:

$$A_v(s) = \frac{v_{out}}{v_{in}} \approx A_o \frac{(1 + \frac{s}{-z_1})(1 + \frac{s}{-z_2})}{(1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 + b_5 s^5)}, \tag{3.5}$$

where

$$A_o = g_{m_1} R_1 g_{m_2} R_2 g_{m_P} R_{out}, \tag{3.6}$$

$$z_1 = -\frac{1}{R_a C_a}, \tag{3.7}$$

$$z_2 = -\frac{1}{R_{cc} C_{cc}}, \tag{3.8}$$

$$C_2' \approx C_2 + g_{m_P} R_{out} C_m \cong C_{GS_P} + g_{m_P} R_{out} (C_{GD_P} + C_m), \tag{3.9}$$

$$b_1 \cong R_a C_a + R_2 C_2' + g_{m_P} R_{out} g_{m_2} R_2 R_1 C_a, \tag{3.10}$$

$$b_2 \cong R_a C_a R_2 C_2' + g_{m_P} R_{out} g_{m_f} R_2 R_a C_a R_{cc} C_{cc}, \tag{3.11}$$

$$b_3 \cong R_2 C_2' R_{cc} C_{cc} R_a C_a + R_2 C_2' R_a C_a R_{out} C_{out}, \tag{3.12}$$

$$b_4 \cong R_2 C_2' R_{cc} C_{cc} R_a C_a R_{out} C_{out} + R_1 C_1 R_2 C_2' R_{cc} C_{cc} R_a C_a, \tag{3.13}$$

$$b_5 \cong R_1 C_1 R_2 C_2' R_{cc} C_{cc} R_a C_a R_{out} C_{out}. \tag{3.14}$$

The LDO simplified small signal model yielded two zeros and five poles. Initially, this might indicate that the stability is in jeopardy. However, the key to the design is to place the poles and zeros so that the behavior of the circuit resembles the one of a two-pole system and, in turn, achieve stability by pole splitting. In general terms, since the b_5 coefficient is extremely lower than the rest of them, the fifth pole always falls at least five decades further than the UGF of the LDO. Consequently, it does not affects the stability of the system and can be neglected from the analysis, which renders a reduced denominator:

$$B(s) \approx 1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4. \tag{3.15}$$

On that account, the two zeros should cancel out two of the poles in order to attain a two-pole system. This becomes a more complicated task when dealing

with light loads due to the fact that two non-dominant pole usually are allocated in high proximity to the UGF. Therefore, it is best to analyze and understand the transfer function particularities at different load scenarios. As it will be detailed later on, depending of the nature of the load current (heavy, medium or light), a certain predominance appear in the denominator coefficients that allows for further simplification.

- **Heavy-load condition** (above 5 mA): Due to the large load current, g_{m_P} is large and R_{out}, quite small, which indicates that the power transistor falls into the linear region. In this scenario, the denominator coefficients are rewritten as

$$b_1 \approx R_a C_a, \tag{3.16}$$

$$b_2 \approx R_a C_a R_2 C_2', \tag{3.17}$$

$$b_3 \approx R_2 C_2' R_{cc} C_{cc} R_a C_a, \tag{3.18}$$

$$b_4 \approx R_2 C_2' R_{cc} C_{cc} R_a C_a R_{out} C_{out}. \tag{3.19}$$

Assuming $R_a C_a \gg R_{out} C_{out}$ and $R_a C_a \gg R_{cc} C_{cc}$, the LDO transfer function at heavy-load condition can be expressed as

$$A_{v_{HL}}(s) \approx A_o \frac{(1 + R_a C_a s)(1 + \frac{1}{-z_2} s)}{(1 + R_a C_a s)(1 + \frac{s}{-p_{dom}})(1 + \frac{s}{-p_1})(1 + \frac{s}{-p_2})},$$

$$A_{v_{HL}}(s) \approx A_o \frac{(1 + \frac{1}{-z_2} s)}{(1 + \frac{s}{-p_{dom}})(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})}, \tag{3.20}$$

where p_{dom} stands for dominant pole, and p_1, p_2 and z_3, for first non-dominant pole, second non-dominat pole and second zero, respectively. In this scenario, the following applies:

$$z_2 = -\frac{1}{R_{cc} C_{cc}}, \tag{3.21}$$

$$p_{dom} = -\frac{1}{R_2 C_2'}, \tag{3.22}$$

$$p_1 = -\frac{1}{R_{cc} C_{cc} [\frac{R_a C_a}{R_a C_a - R_2 C_2'}]}, \tag{3.23}$$

$$p_2 = -\frac{1}{R_{out}C_{out}[1 - \frac{R_2C_2'}{R_aC_a}]}. \tag{3.24}$$

From (3.23) and (3.24), it can be noticed that as the load current decreases, both p_1 and p_2 decrease. The abatement of p_2 is an undesired effect since, if located close enough to the UGF, it could compromise stability. However, this situation will never arise due to the fact that $R_{out}C_{out}$ is very small. As a result, p_2 falls far beyond the UGF. Similarly, p_1 is allocated after the UGF, but at a much closer distance. In order to ensure high stability, a zero-pole cancellation must be established between p_1 and z_2. Usually, the LDO is designed so that it achieves ideal zero-pole cancellation at full-load condition. Therefore, p_1 is initially located at the same frequency as z_2, and then starts to pull away from it and closer to the UGF as the load current diminishes. The non-ideal zero-pole cancellation may render a non entirely smooth gain and phase responses; nonetheless, it does not compromise the stability of the circuit.

- **Medium-load condition** (between 5 mA and 0.5 mA): The power transistor falls out of the linear region, and the system starts working as a three-stage amplifier. Thus, though g_{m_P} decreases, it is still higher than g_{m_1} and g_{m_2}. Hence, the $g_{m_P}R_{out}$ factor increases. Moreover, R_aC_a starts to drop and R_2C_2' to rise. The denominator coefficients can be approximated as

$$b_1 \cong R_aC_a + R_2C_2' + g_{m_P}R_{out}g_{m_2}R_2R_1C_a, \tag{3.25}$$

$$b_2 \approx R_aC_aR_2C_2', \tag{3.26}$$

$$b_3 \approx R_2C_2'R_{cc}C_{cc}R_aC_a, \tag{3.27}$$

$$b_4 \approx R_2C_2'R_{cc}C_{cc}R_aC_aR_{out}C_{out}. \tag{3.28}$$

Assuming $R_aC_a > R_2C_2' \gg R_{out}C_{out}$ and $R_aC_a \gg R_{cc}C_{cc}$, the LDO transfer function at medium-load condition is rewritten as

$$A_{v_{ML}}(s) \approx A_o\frac{(1 + R_aC_as)(1 + \frac{1}{-z_2}s)}{(1 + R_aC_as)(1 + \frac{s}{-p_{dom}})(1 + \frac{s}{-p_1})(1 + \frac{s}{-p_2})},$$

$$A_{v_{ML}}(s) \approx A_o\frac{(1 + \frac{1}{-z_2}s)}{(1 + \frac{s}{-p_{dom}})(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})}, \tag{3.29}$$

where

$$z_2 = -\frac{1}{R_{cc}C_{cc}}, \tag{3.30}$$

$$p_{dom} = -\frac{1}{R_2C_2' + g_{m_P}R_{out}g_{m_2}R_2R_1C_a}, \tag{3.31}$$

$$p_1 = -\frac{1}{R_{cc}C_{cc}[\frac{R_aC_a}{R_2C_2' - R_{out}C_{out}}]}, \tag{3.32}$$

$$p_2 = -\frac{1}{R_{out}C_{out}[\frac{R_2C_2' - R_{out}C_{out}}{R_aC_a}]}. \tag{3.33}$$

From (3.32) and (3.33), it can be inferred that as the load current decreases, p_1 increases and p_2 decreases. Once again, the increment of p_2 is an unpleasant side effect. However, since $R_{out}C_{out}$ is still quite small, this scenario will never take place. Therefore, despite its growing tendency, p_2 falls relatively far from the UGF. On the other hand, p_1 starts off behind z_2, and then begins to get closer to it as the load current lessens. Throughout the entire medium-load range, the zero-pole cancellation between p_1 and z_2 is not ideal, which, as mentioned before, might end up causing a non-flat frequency response.

- **Light-load condition** (below 0.5 mA): The small load current drives the power transistor to work in weak inversion until eventually reaching the cut-off region. Hence, g_{m_P} abates and R_{out} becomes quite large. Thus, the $g_{m_P}R_{out}$ factor experiences a large augmentation. On the contrary, R_aC_a diminishes. In this scenario, the denominator coefficients are abbreviated as

$$b_1 \cong R_2C_2' + g_{m_P}R_{out}g_{m_2}R_2R_1C_a, \tag{3.34}$$

$$b_2 \approx R_aC_aR_2C_2', \tag{3.35}$$

$$b_3 \approx R_2C_2'R_{cc}C_{cc}R_aC_a, \tag{3.36}$$

$$b_4 \approx R_2C_2'R_{cc}C_{cc}R_aC_aR_{out}C_{out}. \tag{3.37}$$

Assuming $R_aC_a \geq R_2C_2$, $R_2C_2' \gg R_{cc}C_{cc}$ and $R_2C_2' \gg R_{out}C_{out}$, the LDO transfer function at light-load condition is reduced to

$$A_{v_{LL}}(s) \approx A_o\frac{(1 + R_aC_as)(1 + \frac{1}{-z_2}s)}{(1 + \frac{s}{-p_{dom}})(1 + R_aC_as)(1 + \frac{s}{-p_1})(1 + \frac{s}{-p_2})},$$

$$A_{v_{LL}}(s) \approx A_o \frac{(1+\frac{1}{-z_2}s)}{(1+\frac{s}{-p_{dom}})(1+\frac{s}{p_1})(1+\frac{s}{p_2})}, \tag{3.38}$$

where

$$z_2 = -\frac{1}{R_{cc}C_{cc}}, \tag{3.39}$$

$$p_{dom} = -\frac{1}{R_2C_2' + g_{m_P}R_{out}g_{m_2}R_2R_1C_a}, \tag{3.40}$$

$$p_1 = -\frac{1}{R_{cc}C_{cc}[\frac{R_aC_a}{R_2C_2'-R_{out}C_{out}}]}, \tag{3.41}$$

$$p_2 = -\frac{1}{R_{out}C_{out}[\frac{R_2C_2'-R_{out}C_{out}}{R_aC_a}]}. \tag{3.42}$$

From (3.41) and (3.42), it can be observed that the behavior of the two non-dominant poles (p_1 and p_2) is the same as the one of the medium-load condition. The rising trend of p_2 becomes more critical in this scenario, since it starts to get much closer to the UGF. Nevertheless, the idea is to design the circuit so that p_2 remains far enough from it to achieve stability. On the contrary, p_1 starts to get much closer to z_2. It is best to design the LDO so that the ideal zero-pole cancellation between p_1 and z_2 occurs at no-load condition.

In order to have a better understanding of the behavior of the LDO at different load conditions, a sketch of the pole-zero mapping for each scenario has been drawn. However, in order to facilitate the visualization, it is best to change pole-zero notation: p_5 represents the fifth pole that always falls far beyond the UGF; p_{out}, the pole inversely correlated to $R_{out}C_{out}$; p_{cc}, the pole inversely correlated to $R_{cc}C_{cc}$; p_2, the pole inversely correlated to R_2C_2'; p_a, the pole inversely correlated to R_aC_a; z_a, the zero inversely correlated to R_aC_a; and finally, z_{cc}, the zero inversely correlated to $R_{cc}C_{cc}$.

Figure 3.7 shows an approximation of the pole-zero mapping of the LDO at each load condition, following the new established pole-zero notation. At heavy-load condition (Figure 3.7(a)), it can be observed that p_a and z_a start off at very low frequencies, and then start to increase. Meanwhile p_2, which becomes the dominant pole (p_{dom}), starts to decrease and pull closer to them. Furthermore, p_{cc} is initially canceled out by z_{cc}. However, it begins to pull away from it, and closer to the UGF. Additionally, p_{out} is located far away from the UGF. It starts to move closer to it as the load decreases, nonetheless. Finally, p_5 falls even further away from the UGF. At medium-load condition (Figure 3.7(b)), p_a and z_a start off further away from the origin of the LHP, and following the same trend as before. Similarly, p_2 remains

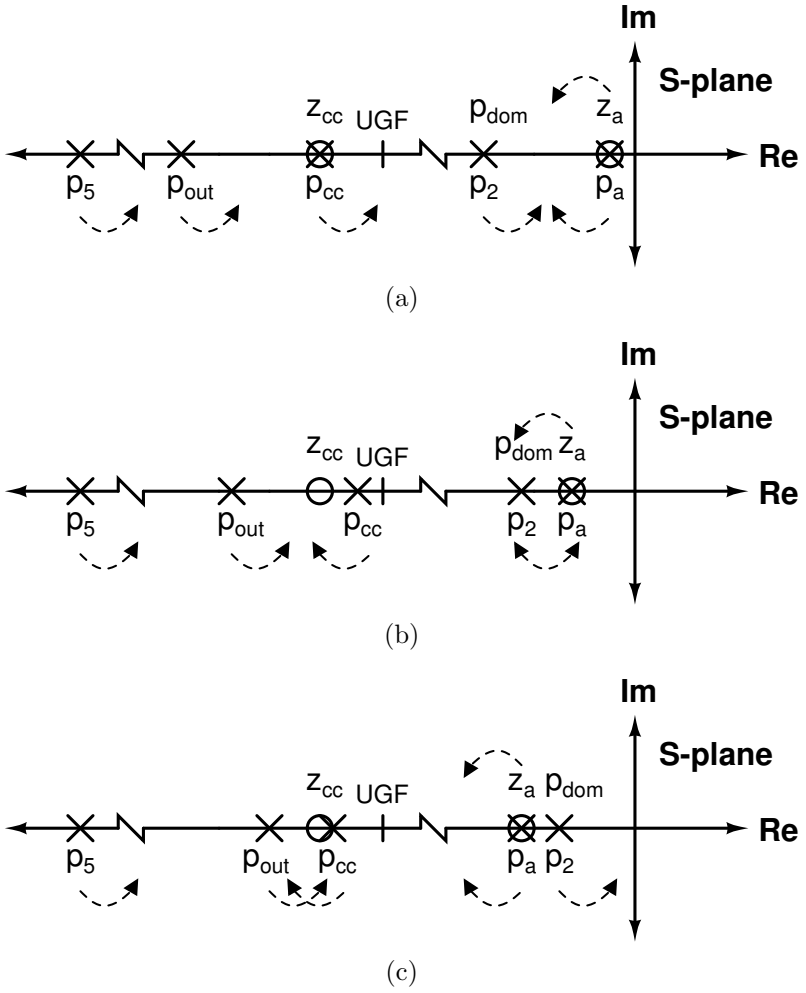


Figure 3.7: Pole-zero mapping of the LDO. (a) Heavy-load condition. (b) Medium-load condition. (c) Light-load condition.

on the same track as before as well, and moves even closer to p_a and z_a. On the contrary, p_{cc} starts off very close to the UGF and then begins to move back to the location of z_{cc}. In addition to that, p_{out} starts to get much closer to the UGF as the load current reduces. Finally, once again p_5 is located quite far from the UGF. At light-load condition (Figure 3.7(c)), p_a and z_a eventually switch locations with p_2, as it was expected due to the its increasing and decreasing tendencies, respectively. Moreover, p_{cc} keeps on moving closer to z_{cc} until it finally reaches it and achieve ideal zero-pole cancellation. Additionally, p_{out} gets much closer to the UGF as the load current abates, reaching its lowest value at no-load condition. Finally, p_5 is much closer to the UGF than before, but still pretty far from the rest of the poles of the system.

3.3 Large Signal Analysis

Large signal analysis entails a study of the transient response of the LDO, when the behavior of the circuit falls out of its steady state. In these fully integrated LDOs, the main SR limiter is the gate capacitance of the power transistor (C_2'). Therefore, understanding the charge/discharge behavior of this capacitor is essential. Figure 3.8 shows how the circuit responds to sudden variations in the load current.

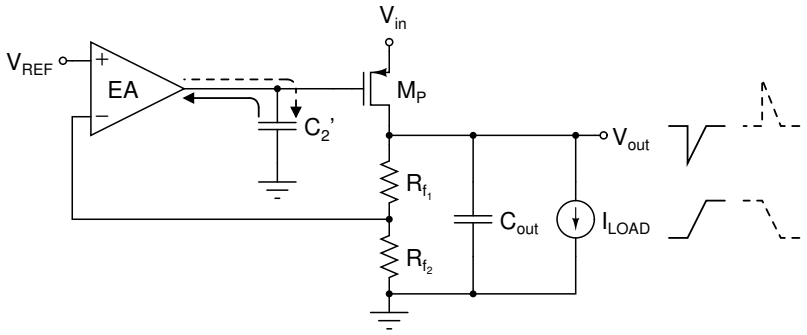


Figure 3.8: Transient response of the LDO.

As it can be visualized, the circuit reacts differently to rising and falling load current (I_{LOAD}) variations. When a sudden increment occurs (solid line), V_{out} drops momentarily due to the extra amount of charge suddenly injected, which causes C_2' to discharge by pushing current into the EA. On the contrary, when a sudden abatement takes place (dashed line), V_{out} rises temporarily in order to compensate the sudden lack of charge, which causes C_2' to pull current from the EA for charging purposes. Thus, the higher the current the EA is able to push/pull to/from C_2', the faster the LDO becomes.

As mentioned before, the EA selected for this implementation was class AB op-amp. This circuit features a push-pull network output stage, as it is shown in Figure 3.9. In this depiction, V_G stands for the gate voltage of M_P.

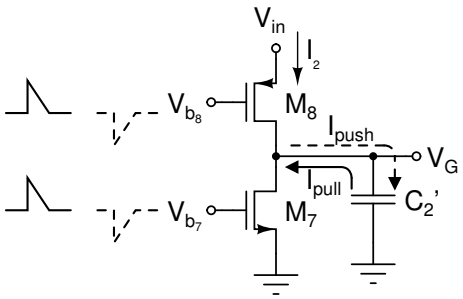


Figure 3.9: Push-pull output stage of the EA.

As it can be noticed, the steady-state current of the output stage is I_2, which becomes the minimum charge/discharge current of C_2'. Therefore, a high I_2 renders

a fast LDO and reduces the voltage peaks of V_{out}. Furthermore, the behavior of the push-pull network is quite simple: when C_2' needs to discharge (solid line), V_{b_8} drops temporarily driving M_8 to the cut-off region. This leaves M_7 as the discharge load of C_2'. Meanwhile, V_{b_7} rises momentarily to pull even more current from C_2' and aid in the discharge time reduction. On the other hand, when C_2' needs to be charged (dashed line), V_{b_7} drops briefly and sends M_7 to the cutt-off region, which yields C_2' as the sole load of M_8. Simultaneously, V_{b_8} augments momentarily in order to push more current to charge C_2'. The equations of I_{push} and I_{pull} are detailed below:

$$I_{push} \approx I_2 + g_{m_8}\Delta V_{b_8} = I_2 + \sqrt{2I_2\mu_p C_{ox}(\frac{W}{L})_8}\Delta V_{b_8}, \tag{3.43}$$

$$I_{pull} \approx I_2 + g_{m_7}\Delta V_{b_7} = I_2 + \sqrt{2I_2\mu_n C_{ox}(\frac{W}{L})_7}\Delta V_{b_7}, \tag{3.44}$$

where ΔV_{b_7} and ΔV_{b_8} stand for the transitory voltage variation of the bias voltage of M_7 and M_8, correspondingly. Figure 3.10 depicts the entire EA and shows how V_{b_7} and V_{b_8} are generated. In this picture, V_{fb} represents the feedback voltage generated by the resistor network from V_{out}.

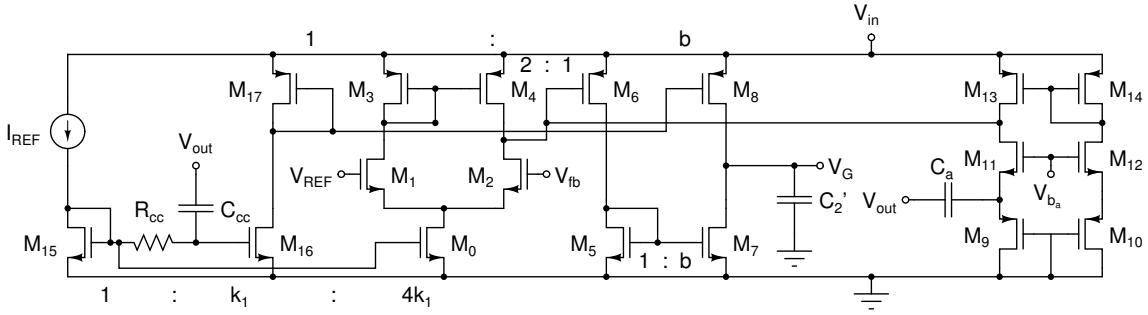


Figure 3.10: Schematic of the error amplifier.

As it can be visualized, V_{b_7} is provided by the active feedback block (C_a and transistors M_9-M_{14} and M_5-M_6), whereas V_{b_8} is generated by the dynamic biasing one (C_{cc}, R_{cc} and transistors M_{15}-M_{17}). Both paths work similarly: a high-pass filter is implemented by a capacitor and a resistor (or a transistor acting as a resistor), thus sensing the voltage spikes of V_{out}. These voltage spikes are fed back to the circuit and slightly amplified so that the output stage is able to draw more current during the sudden transient variations. The expressions for the voltage spikes are found as

$$\Delta V_{b_7} \approx 2I_5 C_{ox}\sqrt{\mu_p\mu_n(\frac{W}{L})_5(\frac{W}{L})_6}\Delta V_{out}, \tag{3.45}$$

$$\Delta V_{b_8} \approx 2I_{16}C_{ox}\sqrt{\mu_p\mu_n(\frac{W}{L})_{16}(\frac{W}{L})_{17}}\Delta V_{out}, \tag{3.46}$$

where $I_5 = I_6$ and $I_{16} = I_{17}$, which correspond to the currents of transistors M_5, M_6, M_{16} and M_{17}, respectively. Expressions (3.45) and (3.46) are linear approximations. The accuracy for the V_{b_7} equation is degraded due to the fact that is generated by the active feedback block, where a transistor (non-linear element) is employed as a resistor for the filter. More on the topic, the use of different paths ultimately causes asymmetry between the responses to negative (solid line) and positive (dashed line) output slewing periods of V_{out}. The current mirrors ratios (k_1 and b) shown in Figure 3.10, along with expressions (3.43) through (3.46) allow for a more precise description:

$$I_{push} \approx k_1 b I_{REF}(1 + 2k_1\mu_p C_{ox}(\frac{W}{L})_{17}\sqrt{2k_1 I_{REF}\mu_n C_{ox}(\frac{W}{L})_{15}}\Delta V_{out}), \tag{3.47}$$

$$I_{pull} \approx k_1 b I_{REF}(1 + 2k_1\mu_n C_{ox}(\frac{W}{L})_{5}\sqrt{2I_{REF}\mu_p C_{ox}(\frac{W}{L})_{15}}\Delta V_{out}). \tag{3.48}$$

Equations (3.47) and (3.48) can be further simplified to attain a better understanding of the difference between positive and negative output slewing responses:

$$I_{push} \approx k_1 b(I_{REF} + \sqrt{k_1}g_{m_{17}}^2 g_{m_{15}}\Delta V_{out}), \tag{3.49}$$

$$I_{pull} \approx k_1 b(I_{REF} + \sqrt{\frac{\mu_p}{\mu_n}}g_{m_5}^2 g_{m_{15}}\Delta V_{out}). \tag{3.50}$$

Thus, it can be inferred from (3.49) and (3.50) that the negative slewing response falls behind compared to the positive one, and therefore requires additional compensation. On that account, an extra SRE block was implemented, whose main transconductor and behavior are illustrated in Figure 3.11.

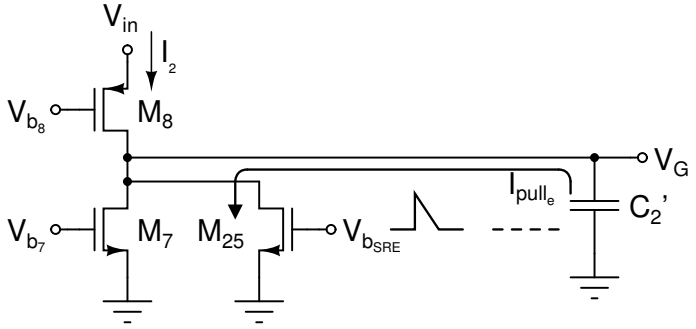


Figure 3.11: Output transconductor of the SRE block.

It can be easily inferred that M_{25} is the output transconductor of the SRE. Moreover, this transistor works in the cut-off region at the steady-state, unlike M_7 and M_8 which draw a steady-state current (I_2). During the negative output slewing (solid line), the bias voltage of M_{25} ($V_{b_{SRE}}$) rises in order to pull an extra current from C_2' (I_{pull_e}) and speed up the discharge. During the positive output slewing (dashed line), M_{25} remains inactive. Whenever active, M_{25} will work in the triode region. Hence, the linear approximation of the extra pull current can be found as

$$I_{pull_e} \approx \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_{25}[(\Delta V_{b_{SRE}} - V_{TH_n})]V_G, \tag{3.51}$$

where $\Delta V_{b_{SRE}}$ stands for the full range variation of $V_{b_{SRE}}$, which usually starts off at the range of few milivolts in order to drive M_{25} to the cut-off region. Figure 3.12 illustrates how $V_{b_{SRE}}$ is generated.

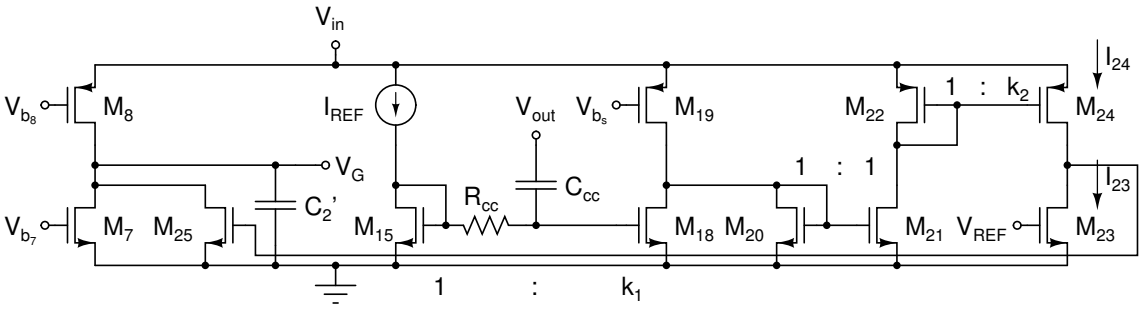


Figure 3.12: Schematic of the SRE block.

As it can be noticed, the dynamic biasing block (R_{cc}, C_{cc} and transistor M_{15}) is used once more as a high-pass filter and node watcher. A current substracter (transistors M_{18} and M_{20}) is utilized to generate an opposite reaction to the voltage spikes that appear in V_{out} and appropriately compensate the transient response. Transistors M_{23} and M_{24} are in charge of triggering M_{25}. In order to keep the latter in the cut-off region at steady-state, M_{23} has to be pushed to the triode region and M_{24}, to saturation. The condition to be met to guarantee this scenario is $I_{24} > I_{23}$. Furthermore, the higher I_{24} gets, the larger $\Delta V_{b_{SRE}}$ becomes, which, in turn, implies that more transient current is injected to M_{25}. Therefore, the ratios (k_1 and k_2) of the current mirrors determines I_{pull_e}. The expression for the transient variation of I_{24} is established as

$$\Delta I_{24} \approx g_{m_{24}}\Delta V_{gs_{24}} = k_1 k_2 g_{m_{18}}\Delta V_{gs_{24}} = k_1 k_2\sqrt{2I_{REF}\mu_p C_{ox}(\frac{W}{L})_{18}}\Delta V_{gs_{24}}, \tag{3.52}$$

where

$$\Delta V_{gs_{24}} \approx 2k_1 k_2 I_{REF} C_{ox}(\frac{W}{L})_{22}\sqrt{\mu_p\mu_n}\Delta V_{out}. \tag{3.53}$$

So, replacing (3.53) in (3.52) renders

$$\Delta I_{24} \approx 2k_1^2 k_2^2 I_{REF} \mu_p C_{ox} (\frac{W}{L})_{22} \sqrt{2 I_{REF} \mu_n C_{OX} (\frac{W}{L})_{18}} \Delta V_{out}, \tag{3.54}$$

which can also be rewritten as

$$\Delta I_{24} \approx k_1 k_2 g_{m_{22}}^2 g_{m_{18}} \Delta V_{out}. \tag{3.55}$$

Ultimately, the actual variation of $V_{b_{SRE}}$ can be found as

$$\Delta V_{b_{SRE}} \approx \Delta I_{24} R_{ON_{23}} \approx k_1 k_2 g_{m_{22}}^2 g_{m_{18}} R_{ON_{23}} \Delta V_{out}, \tag{3.56}$$

where

$$\Delta R_{ON_{23}} \approx \frac{2}{\mu_n C_{ox} V_{OV_{23}} (\frac{W}{L})_{23}} = \frac{2}{\mu_n C_{ox} (V_{REF} - V_{TH_n}) (\frac{W}{L})_{23}}. \tag{3.57}$$

In this case, $V_{OV_{23}}$ represents the overdrive voltage of M_{23}. From (3.56) it can be noticed that $g_{m_{18}}$ and specially $g_{m_{22}}$ basically determine $\Delta V_{b_{SRE}}$, and therefore should be as large as possible without compromising the power consumption.

Besides the amount of transient current generated, the speed of the circuit is critical as well. The response time of the SRE block depends essentially on how fast the circuit is able to activate M_{25}. Thus, the expression for the response time is found as

$$t_{resp_{SRE}} = \frac{\Delta V_{ON_{25}} C_{p_{25}}}{\Delta I_{24}} \approx \frac{(V_{TH_n} - V_{OV_{23}}) C_{p_{25}}}{k_1 k_2 g_{m_{22}}^2 g_{m_{18}} \Delta V_{out}}, \tag{3.58}$$

where $C_{p_{25}}$, the parasitic capacitance at the gate of M_{25}. It can be deduced from (3.58 that the response time increases with $C_{p_{25}}$, which is not desirable. Consequently, $(\frac{W}{L})_{25}$ should be kept low in order to augment the speed of the SRE block. Furthermore, enlarging $g_{m_{22}}$ and $g_{m_{18}}$ - specially the former due to its inverse quadratic correlation - while maintaining the power consumption at a minimum seems to be the best practice to reduce the response time.

Finally, the size of the voltage peaks of the output voltage can be estimated as well. Recalling Figure 3.8, the negative output slewing (solid line) constitutes an undershoot, and the positive one (dashed line), an overshoot. The appearance of these voltage spikes is caused by the sudden charge shift that C_{out} experiences. When I_{LOAD} suddenly rises, M_P is not able to provide the current immediately. Therefore, C_{out} starts to discharge in order to deliver the current to the load, which causes V_{out} to drop. On the other hand, when I_{LOAD} falls abruptly, M_P is incapable of turning off its current instantaneously. This leaves C_{out} overcharged, which translates to an increment of V_{out}. Thus, The push-pull network and the SRE block are put in place to compensate for the lack/excess of charge through V_G. At any given time, the

following applies:

$$\Delta I_{SD_P} \approx -g_{m_P} \Delta V_G g_{m_P}, \tag{3.59}$$

where ΔI_{SD_P} stands for the variation of the source-drain current of M_P. Likewise, the magnitude of any output voltage spike (ΔV_{out}) can be expressed as

$$\Delta V_{out} \cong \frac{|\Delta I_{LOAD} - \Delta I_{SD_P}| t_{resp_L}}{C_{out}}, \tag{3.60}$$

where t_{resp_L} represents the time required for the entire loop to react. Relaying on the push an pull currents found above, the expressions for both the maximum undershoot (ΔV_{out_N}) and overshoot (ΔV_{out_P}) are found as

$$\Delta V_{out_N} \approx \frac{|I_{max} - g_{m_P}(I_{pull} + I_{pull_e}) R_2| t_{resp_L}}{C_{out}}, \tag{3.61}$$

$$\Delta V_{out_P} \approx \frac{|I_{max} - g_{m_P}(I_{push}) R_2| t_{resp_L}}{C_{out}}, \tag{3.62}$$

where I_{max} represents the maximum load current. It is important to mention that g_{m_P} will vary for each case, since the M_P starts off at different regions of operation.

3.4 Transistor Dimensioning

The specifications of the LDO set the tone for the design process, which may vary depending on the application. The main specs established for this design are detailed in Table 3.1.

Table 3.1: LDO specifications.

Maximum Load Current ($\mathbf{I_{max}}$)	$50\ mA$
Preset Output Voltage ($\mathbf{V_{out}}$)	$1.8\ V$
Dropout Voltage ($\mathbf{V_{DO}}$)	$200\ mV$
Output Capacitance ($\mathbf{C_{out}}$)	$50\ pF$
Quiescent Current ($\mathbf{I_Q}$)	$< 100\ \mu A$
Power Supply Rejection Ratio (PSRR)	$\leq -40\ dB$ @ $10\ kHz$
Phase Margin at no-load condition ($\mathbf{PM_{nl}}$)	$\geq 60°$
Load Current Shift Period ($\mathbf{\Delta t_s}$)	$1\ \mu s$
Voltage Spikes ($\mathbf{\Delta V_{out}}$)	$\leq 200\ mV$

With V_{DO} and I_{max} established the following can be found:

$$R_{ON_P} = \frac{V_{DO}}{I_{max}}. \tag{3.63}$$

Once R_{ON_P} is found, the aspect ratio of M_P ($(\frac{W}{L})_P$) and, consequently, g_{m_P} are

deduced. Furthermore, the parasitic capacitances (C_2) of M_P are also established. Similarly, once I_Q is set, the values of R_{f_1} and R_{f_2} are found, which in turn set the value of R_{out} at no-load condition. For this particular design I_Q was set to 60 μA.

$$R_{out} = \frac{1}{\frac{1}{R_{f_1}+R_{f_2}} + \frac{1}{R_{LOAD}} + G_{DS_P}}. \tag{3.64}$$

Generally the reference current (I_{REF}) that powers the entire circuit comes from a preset voltage reference. Thus, it is customary to set said curren to a generic value and use a unitary transistor ($\frac{W}{L} = 1$) as the source for the current mirror. Thus, the aspect ratio of M_{15} is easily found, which subsequently leads to $g_{m_{15}}$. In this case, I_{REF} is 1 μA.

For an ideal one-pole system, the gain-bandwidth (GBW) and the UGF are the same. Thus, in order to facilitate the design process, this equivalence is utilized. The GBW is defined as

$$GBW = A_o p_{dom} \cong \frac{k_1 b g_{m_{15}}^2 g_{m_P} R_{out}}{\lambda I_{REF} C_2'}. \tag{3.65}$$

Hence, if a value is assigned to C_m and assuming a UGF of 1.5 MHz, the product of the current mirror ratios can be isolated. For this design, C_m was set to 3 pF. The trade-off between area (C_2') and power consumption ($k_1 b$) is clearly portraited in (3.65).

$$k_1 b = \frac{GBW \lambda I_{REF} C_2'}{g_{m_{15}}^2 g_{m_P} R_{out}}. \tag{3.66}$$

It is best to set the value of ΔV_{out} a bit lower than the constrain given by the specs. This will allow the circuit to perform within the confines of the specs even when experiencing PVT variations. For this design, ΔV_{out} was set to 150 mV. From this spec the value of I_{push} can be found by recalling equation (3.62). Once I_{push} is found, the use of expression (3.49) will render k_1 as

$$k_1 \approx (\frac{I_{push} - k_1 b I_{REF}}{\frac{\mu_n}{\mu_p} g_{m_{15}}^3 \Delta V_{out}})^{2/3}. \tag{3.67}$$

With k_1 established, b is deduced as well. In a similar way, recalling (3.48) and (3.61) I_{pull} and I_{pull_e} are found, respectively. The latter is always considerabily larger than the former, due to the small value of g_{m_P} at no-load condition. Moreover, using (3.51),(3.56) and (3.58) a 2-equation system is established which allows to discover the second current mirror ratio of the SRE (k_2) and the aspect ratio of M_{25} ($(\frac{W}{L})_{25}$):

$$I_{pull_e} \approx \frac{1}{2}\mu_n C_{ox} (\frac{W}{L})_{25} [(k_1^4 k_2 \frac{\mu_p}{\mu_n} g_{m_{15}}^3 \Delta V_{out} - V_{TH_n})] V_G, \tag{3.68}$$

$$t_{resp_{SRE}} \approx \frac{(V_{TH_n} - V_{OV_{23}})C_{p_{25}}}{k_1^4 k_2 \frac{\mu_p}{\mu_n} g_{m_{15}}^3 \Delta V_{out}}. \tag{3.69}$$

The design of the active feedback elements is a bit more complicated. The value of R_a - and g_{m_a} for that matter - changes as the load current varies. Thus, it is best to start by setting the limit values. The most critical one is the no-load scenario, where the PM spec becomes useful. Hence, assuming an ideal pole-zero cancellation between p_{cc} and z_{cc}, the following applies:

$$PM_{nl} = 180° - \arctan\left(\frac{UGF}{-p_2}\right) - \arctan\left(\frac{UGF}{-p_{out}}\right). \tag{3.70}$$

So, recalling equations (3.40) and (3.42), and setting a value to C_a, then R_a at the no-load condition can be found. For this particular design, the selected value for C_a was 3 pF in order to achieve a PM of 63°. Similarly, recalling (3.23) the value of R_a at full-load condition is found by establishing ideal pole-zero cancellation between p_{cc} and z_{cc}. Hence, $R_a C_a \gg R_2 C_2'$, which can be attained by the following relationship:

$$R_a \approx 1000 R_2. \tag{3.71}$$

Once the values of R_a are determined, the adaptive bias voltage generator and the rest of the active feedback circuit is sized and optimized in order to attain them.

The circuit was designed using the IBM 0.18 μm CMOS process design kit (PDK). Its extracted parameters are listed in Table 3.2.

Table 3.2: CMOS extracted parameters.

Triode
$V_{TH_0} = 0.675\ V$
$\theta = 0.1$
Saturation
$V_{TH_0} = 0.62\ V$
$\theta = 0.067$
$k_p = 190.4\ \mu A/V$
$\alpha = 1.34$
$\phi_0 = 0.75\ V$
$\gamma = 0.73\ V^{1/2}$

As it can be noticed, the parameters are generic for both NMOS and PMOS transistors. This may seem confusing since transistors always present different behaviors. This difference usually appears in the V_{TH} and k_p parameters. The latter is defined by the mobility of the transistor: μ_n and μ_p for NMOS and PMOS, respectively. Nevertheless, in this case the distinction between the two of them appears in the developed mathematical models, which are described in Table 3.3.

Table 3.3: CMOS mathematical models.

NMOS	**PMOS**
$V_{TH} = V_{TH_0} + \gamma(\sqrt{\phi_0 - V_{BS}} - \sqrt{\phi_0})$	$V_{TH} = V_{TH_0} - \gamma(\sqrt{\phi_0 - V_{BS}} - \sqrt{\phi_0})$
Triode	**Triode**
$I_{DS} = \frac{W}{L} k_p[(V_{GS} - V_{TH})V_{DS} - \frac{\alpha}{2}V_{DS}^2]$	$I_{DS} = \frac{W}{L} k_p[(V_{GS} - V_{TH})V_{DS} - \frac{\alpha}{2}V_{DS}^2]$
Saturation	**Saturation**
$I_{DS} = \frac{W}{L} \frac{k_p}{2\alpha(1+\theta(V_{GS}-V_{TH}))}(V_{GS} - V_{TH})^2$	$I_{DS} = \frac{W}{L} \frac{k_p}{2\alpha(1-\theta(V_{GS}-V_{TH}))}(V_{GS} - V_{TH})^2$

As it can be observed, the difference in the V_{TH} parameter is established by adding (NMOS) or subtracting (PMOS) the variable factor to or from the intrinsic threshold voltage (V_{TH_0}). Similarly, θ defines the difference at the saturation region by acting as a positive or negative factor. Thus, the model does provide expressions for V_{TH_n} and V_{TH_p}, as well as k_n and k_p.

The schematic of the entire LDO is depicted in Figure 3.13, and the complete design is summarized in Table 3.4.

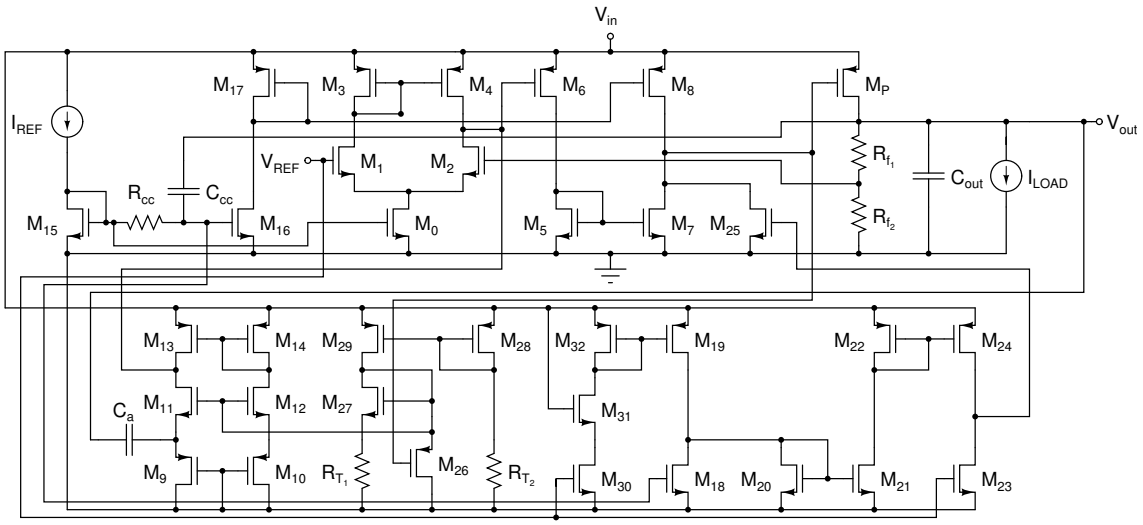


Figure 3.13: Schematic of the LDO.

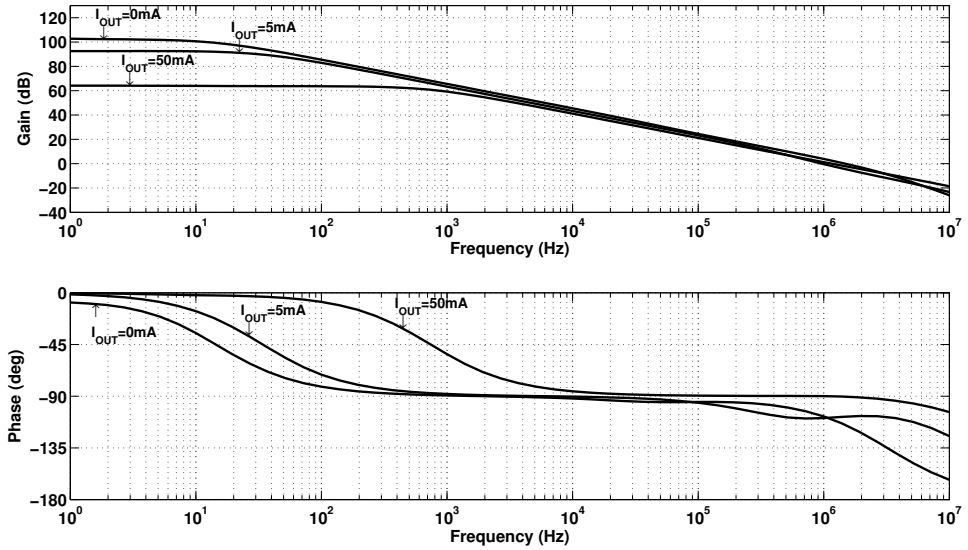
All the elements of the LDO previously described appear clearly in the schematic. The main issue to highlight and elaborate on is the adaptive bias voltage generator of the adaptive active feedback block. This circuit is formed by transistors M_{26} through M_{29}, and by resistors R_{T_1} and R_{T_2}. This circuit receives V_G as the trigger signal since is the one that changes according to the load current. Transistor M_{26} acts as a semi enable/disable transistor of the adaptive active feedback block. When I_{LOAD} is high, V_G is low, which causes M_{26} to draw current and V_{b_a} (gate voltage of M_{27}, M_{11} and M_{12}) to drop. As I_{LOAD} decreases, V_{b_a} increases, which in turn causes R_a to diminish. Once the light-load condition is reached, M_{26} is turned off completely. The resistance are used to set the DC operating point of the circuit and to counteract

the effects of temperature variations. Poly-resistors present a temperature gradient opposite to the transistor one, which makes the circuit temperature-resilient. The design of the resistances and M_{27} is a bit complex since the resistance are quite sensitive to process variations, and the transistor to temperature variations. Hence, a trade-off between the two is established and has to be managed carefully.

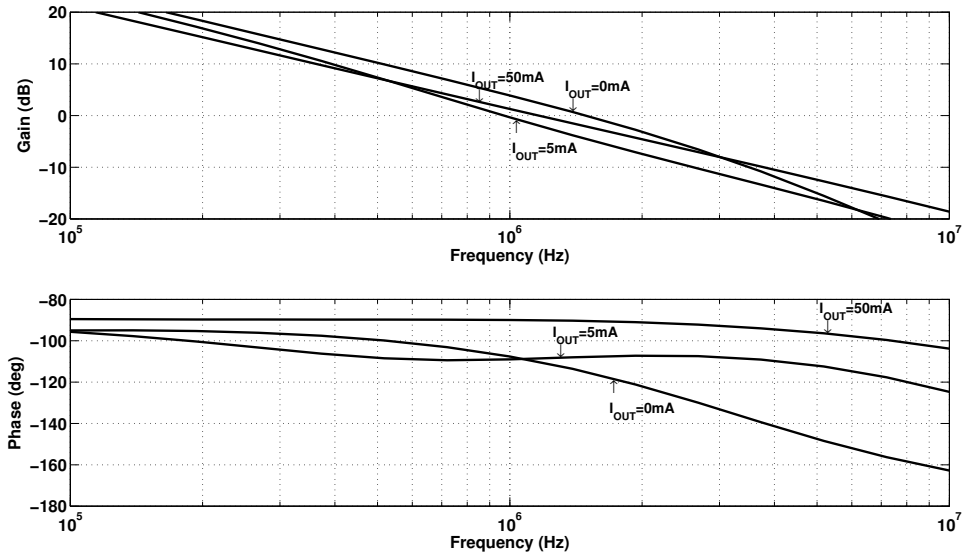
Table 3.4: LDO design.

$\mathbf{M_P}$	$W = 3000\ \mu m$	$L = 0.4\ \mu m$
$\mathbf{M_0}$	$W = 10\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_1}$, $\mathbf{M_2}$	$W = 8.8\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_3}$, $\mathbf{M_4}$, $\mathbf{M_{13}}$, $\mathbf{M_{14}}$, $\mathbf{M_{19}}$, $\mathbf{M_{25}}$	$W = 1.4\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_5}$, $\mathbf{M_6}$, $\mathbf{M_{17}}$, $\mathbf{M_{20}}$, $\mathbf{M_{21}}$, $\mathbf{M_{22}}$, $\mathbf{M_{32}}$	$W = 0.7\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_7}$, $\mathbf{M_8}$	$W = 4.2\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_9}$, $\mathbf{M_{10}}$, $\mathbf{M_{15}}$, $\mathbf{M_{23}}$, $\mathbf{M_{28}}$, $\mathbf{M_{29}}$	$W = 2\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{11}}$, $\mathbf{M_{12}}$	$W = 2.8\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{16}}$, $\mathbf{M_{18}}$	$W = 2.5\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{24}}$	$W = 2.1\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{26}}$	$W = 1\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{27}}$	$W = 67.2\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{30}}$	$W = 0.5\ \mu m$	$L = 2\ \mu m$
$\mathbf{M_{31}}$	$W = 4\ \mu m$	$L = 2\ \mu m$
$\mathbf{C_a}$, $\mathbf{C_m}$	$3\ pF$	
$\mathbf{C_{cc}}$	$0.3\ pF$	
$\mathbf{R_{cc}}$	$90\ k\Omega$	
$\mathbf{R_{f_1}}$	$20\ k\Omega$	
$\mathbf{R_{f_2}}$	$40\ k\Omega$	
$\mathbf{R_{T_1}}$,$\mathbf{R_{T_2}}$	$600\ k\Omega$	
$\mathbf{I_{REF}}$	$1\ \mu A$	
$\mathbf{V_{REF}}$	$1.2\ V$	

In order to verify the design and the analysis performed so far, the small-signal model was simulated on Matlab®. All three load conditions were simulated: $I_{LOAD} = 50\ mA$ for heavy load, $I_{LOAD} = 5\ mA$ for medium load, and $I_{LOAD} = 0\ mA$ for light load. The results are shown in Figure 3.14, and they clearly show that the LDO is stable for all load conditions. The PM achieved for each condition is maintained above 60°. The UGF attained is higher than 1 MHz for all load conditions, except for the medium one. As described in Subsection 3.2, p_{cc} falls behind z_{cc}, which manifests itself in both phase and magnitude responses. In the former, a non-flat behavior appears, and in the latter, the UGF falls behind 1 MHz. However, M_P is working in the saturation region (I-V quadratic correlation) and therefore does not require as high of a loop bandwidth as it does in the linear region. Hence, the transient response is not degraded.



(a)



(b)

Figure 3.14: (a) Open-loop response of the LDO small signal model for different load currents (I_{out}). (b) Zoomed-in viewed around the UGF.

Chapter 4

Layout Design

LDO layout design always present some challenges compared to any other regular circuit. The reason for this is the excessive amount of current that has to be generated and transported through the die. Special considerations must be taken in order to avoid undesired effects, such as electromigration (EM) [23]. Furthermore, the power transistor (M_P) and the compensation capacitors (C_a, C_m and C_{cc}) tend to occupy a large amount of area. Therefore, proper placing and design of these elements is key to reduce the size of the integrated circuit. Additionally, mismatch effects have to be taken under consideration, specially for the resistive feedback network (R_{f_1} and R_{f_2}), in order to minimize the random offset of the preset output voltage (V_{out}). Hence, some particular layout techniques were used on the key elements of the LDO in order to render an integrated circuit able to withstand mismatch effects. On that account, this chapter will illustrate the layout of the aforementioned key elements and will give a description of the layout techniques used to address these issues. Ultimately, the complete layout design is depicted.

4.1 Power Transistor

One of the first elements to analyze while realizing the layout design is the power transistor. Due to its large width (W), the use of fingers comes in handy to make a much more efficient use of the die area. A side effect of this technique is the reduction of the parasitic capacitances associated with said transistor (C_2). Furthermore, the distribution of the extremely high current through several instances reduces the size of the metal paths that connect M_P to the input supply voltage (V_{in}). In this particular design, the power transistor was stripped down to 300 instances of $W = 10\ \mu m$. Ultimately, they were organized to conform 5 instances, each one with 60 fingers of $W = 10\ \mu m$, as it can be observed in Figure 4.1. As it can be observed, transistor chaining is employed to reduced the amount of active area. Thus, source (S) and drain (D) terminals are being shared all throughout each 60 fingers instance.

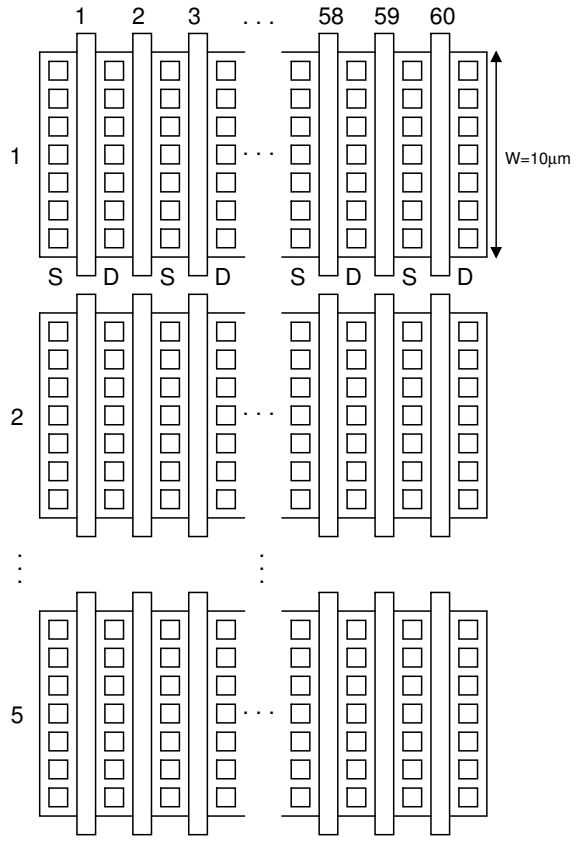


Figure 4.1: Layout design mockup of the power transistor.

Moreover, a large amount of active area contacts are placed to aid even further the current distribution and sheet resistance reduction. On that account, the metal paths that connect M_P to V_{in} and V_{out} should be as wide as possible to further the latter effect. On another topic, routing with polysilicon and diffusion layers should be avoided. Therefore, the gates (fingers) of all 5 instances should be linked together by the first metal layer (M1).

4.2 Differential Pair

The differential pair of the EA (M_1 and M_2) is the only one in the entire LDO, and is the principal element that provides high gain to the loop and thus assures an accurate regulation. Therefore, it is imperative to make its layout design resilient to mismatch effects. The techniques used for this circuit were interdigitation and common centroid [23]. These two techniques ensure that regardless of the orientation and direction of the wafer variation gradient, the symmetry of the differential pair layout design will be maintained at all times. The mockup of the differential pair layout design is illustrated in Figure 4.2. As it can be observed, both transistors were stripped down to 4 instances, each one of $W = 2.1\ \mu m$. The 8 instances are placed

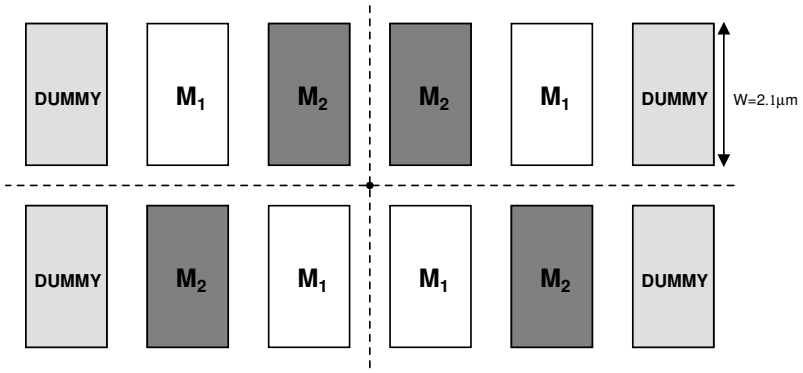


Figure 4.2: Layout design mockup of the differential pair.

so that the design presents complete symmetry. Furthermore, the differential pair is sided by 4 "dummy" transistors. The gradient variation is larger around the border of the wafer, which means that the outer transistors experience larger alterations than the inner ones. Thus, the "dummy" transistors act as a protection wall and conceal the circuit from the more hazardous mismatch effects. Additionally, they provide full symmetry; in other words, each instance will see the same fabrication process layers and imperfections on each side.

4.3 Reference Current Mirrors

The reference current transistor M_{15} receives a current of 1 μA (I_{REF}), and copies to M_{16}, M_0 and M_{18}. Recalling the aspect ratios of these transistors listed in Table 3.4, it can be easily inferred that the ratios of the current mirrors are not whole numbers, but fractionaries. Specifically the cases of M_{16} and M_{18}, the ratio is 1.25, which brings a difficulty in the layout design planing. One way to undertake this complex task and achieve an accurate copy is to stripped down each copy instance into a multiple of a common unitary transistor. Furthermore, this allows to implement interdigitation and common centroid techniques which ensure that the ratio between the reference currents will remain regardless of the presence of fabrication process imperfections. In this particular design, a $W = 0.5\ \mu m$ unitary transistor was chosen. This derived in 4 instances for M_{15}, 5 for M_{16} and M_{18}, and 20 for M_0, as it can be visualized in Figure 4.3. Additionally, it can be perceived that "dummy" transistors are once again utilized to further the resilience of the layout design. They are placed to conform a boundary of the layout design of the actual circuit. Nevertheless, in this particular design one "dummy" transistor is also used as the center of the common centroid array of instances. This resolved the aforementioned issue of fractionary current ratios and ultimately facilitated the layout design.

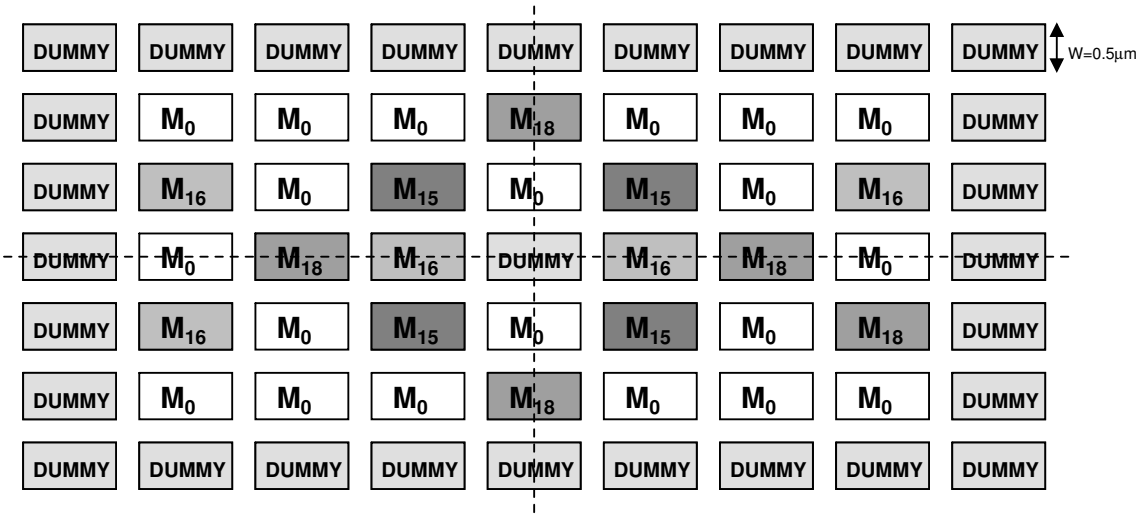


Figure 4.3: Layout design mockup of the reference current mirrors.

4.4 Array of Capacitors

The LDO comprises 3 capacitors in total: C_{cc}, C_m and C_a. The ratio among them is not as critical in terms of performance as it is their stand-alone capacitance value. Process variations and mismatch effects on these elements do introduce some alterations in the frequency response of the circuit. However, most of these alterations are compensated due to the regulated closed loop of the LDO. Nevertheless, a resilient layout design of the capacitors is advised in order to reduce even further the influence of fabrication process imperfections on the performance of the circuit. On that account, techniques such as common centroid and interdigitation come in handy once more. In order to apply them, the larger capacitors (C_m and C_a) have to be stripped down to a common unitary capacitor. In this particular design C_{cc} of 0.3 pF was chosen for this role, thereby rendering 10 instances for both C_m and C_a. The layout design mockup is depicted in Figure 4.4. As it can be visualized, C_{cc} is used as the center of the common centroid array. Moreover, "dummy" capacitors are placed and utilized in the same manner as their transistor equivalent. Furthermore, capacitors are built by an insulator wedged between two metal layers. This means that there is an vertical electric field - and, in turn, vertical charge flow - present between them. Thus, each capacitor is affected by the electric field of its neighbor. Therefore, in order to maintain symmetry in the electric charge flow, each capacitor must see the same electric field at each side, which is where the "dummy" capacitors become useful. A resilient layout design of the capacitors ensures that all the poles and zeros in the transfer function will experience virtually the same frequency allocation shift, and thus will not modify the stability performance indicators of the system.

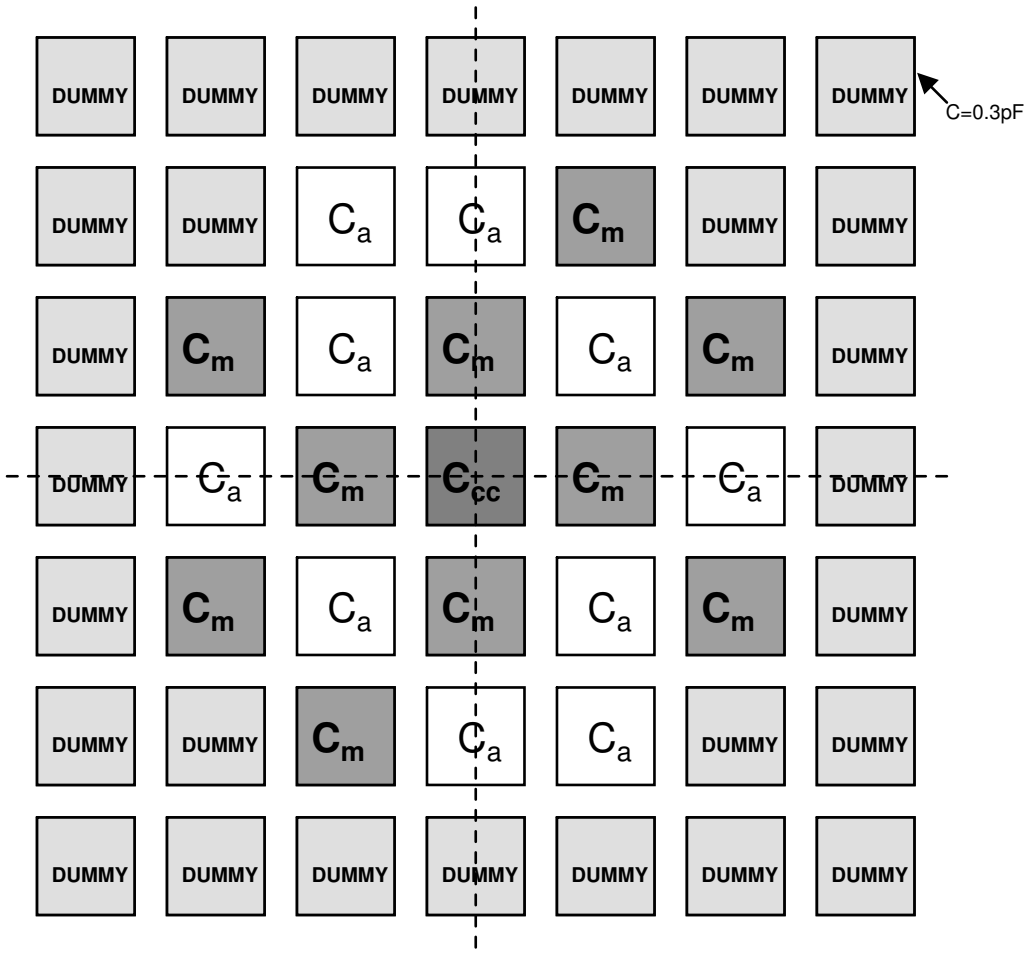


Figure 4.4: Layout design mockup of the array of capacitors.

4.5 Feedback Resistors

Resistors R_{f_1} and R_{f_2} are critical elements in the LDO layout due to the fact that they have a huge impact on the DC operating point of the circuit. Hence, if mismatch effects were to appear between them, a random offset would appear at the output voltage which would degrade the overall performance of the LDO. Consequently, the layout design of these resistors has to be a resilient one, which translate to the use of the already revised techniques of common centroid and interdigitation. Since R_{f_1} represents half of R_{f_2}, it can be implement by an array of two parallel resistors, each one equal to R_{f_2}. The layout design mockup of the feedback resistors is illustrated in Figure 4.5. As it can be noticed, R_{f_2} is used as the center of the common centroid array. Additionally, "dummy" resistors are placed in order to fulfill the role of their transistor and capacitor counterparts. It should be mentioned that the border "dummy" resistors do not need to have the same dimensions as the actual feedback resistors in order to fulfill their role. Hence, as shown in the picture, most of the "dummy" resistors are smaller than the feedback ones. This ultimately saves die

area and allows for a much more efficient layout design. The same techniques were applied to resistors R_{T_1} and R_{T_2} as well. Though they are not as critical as R_{f_1} and R_{f_2}, they do have some impact on the DC operating point.

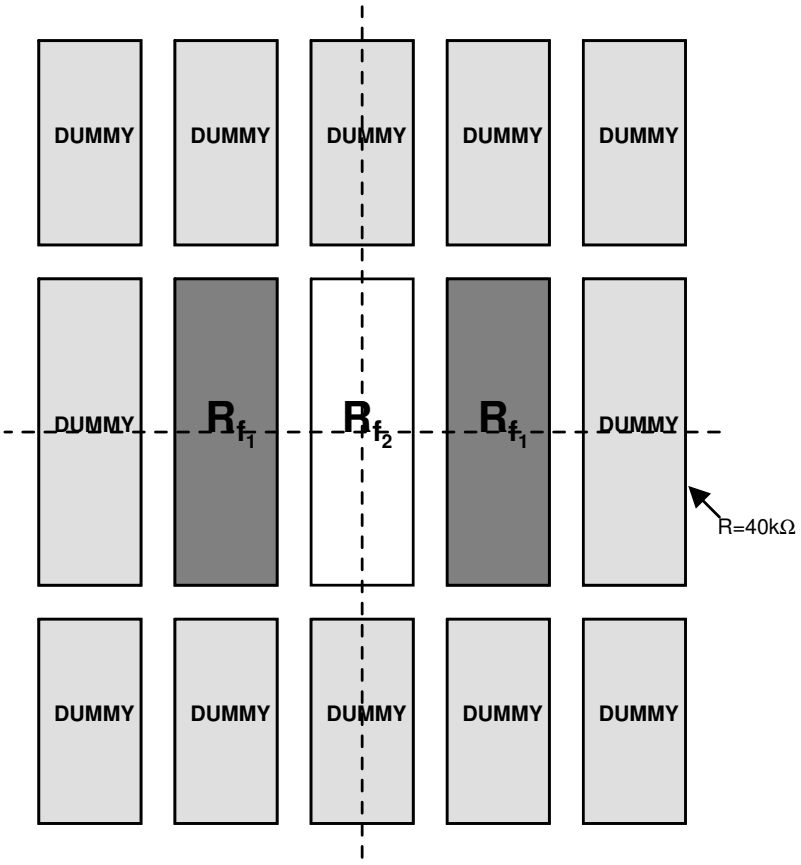


Figure 4.5: Layout design mockup of the feedback resistors.

4.6 LDO Full Layout Design

The complete layout design of the LDO is illustrated in Figure 4.6 and it was developed using Cadence® CAD tools. In order to get a better grasp of the design floorplanning, the main elements have been highlighted on the layout: array of capacitors, feedback resistors, temperature resistors (R_{T_1} and R_{T_2}), power transistor, reference current mirrors, and the differential pair (diff pair).

The power transistor has been placed as near as possible to the input supply voltage ($V_{supp} = V_{in}$) and the output regulated voltage (V_{out}). Furthermore, as mentioned before, the metal paths that connect said transistor to the aforementioned voltage nodes were design to be quite wide. These two precautions were taken in order to attain high signal integrity for the load current (I_{LOAD}). Wide metal paths were employed throughout the layout design according to the current density of each net, both static and dynamic.

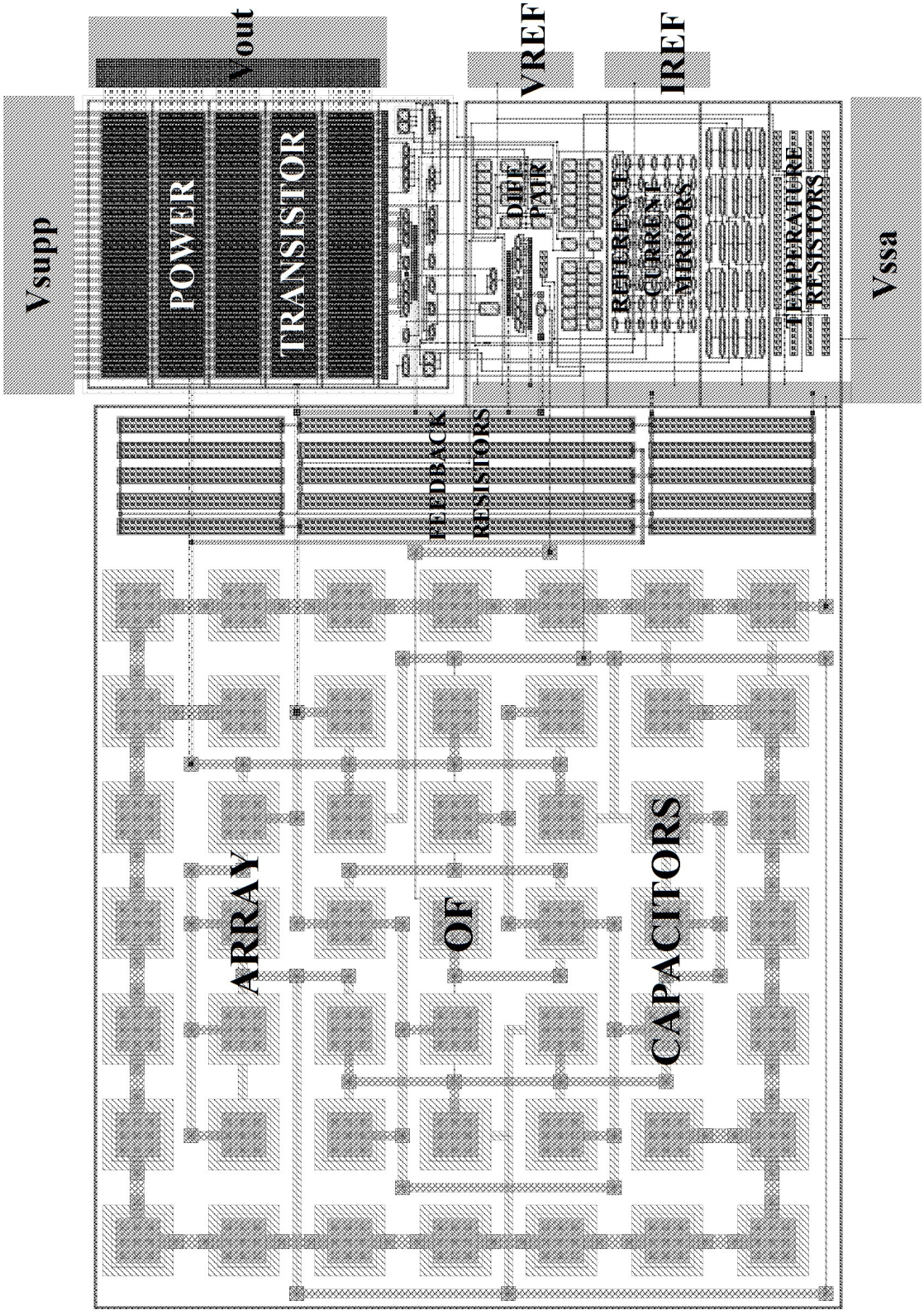


Figure 4.6: Layout design of the LDO.

The array of capacitors, along with the feedback resistors, represent roughly 57% of the entire layout design. In the case of the former, the devices available in

the PDK were implemented using the top layers. The top layer has a much larger minimum width than the rest of them, which derived in a considerably large layout specially due to the complex internal routing of the array. The feedback resistors were implemented by poly-resistors, which tend to be quite large as well for values surpassing 10 $k\Omega$.

There are several guard rings throughout the layout design. Nevertheless, the main guard rings are the ones that separate the P-type devices from the N-type devices. The former is connected to V_{supp} and the latter to V_{ssa}. The other guard rings distribuited within the two main ones are placed in order to maintain a low source to substrate distance for all devices.

Techniques such as common centroid and interdigitation were performed on most of the remaining current mirrors within the LDO. This ensures a high resiliance to gradient variations, which are usually present in the fabrication process.

The final die are was of 295.25 μm $\times$ 209.57 μm = 0.062 mm^2. It is worth mentioning that the power transistor - which usually takes up at least 33% in most LDO layout designs - only takes up aroud 8% of the entire area in this particular design. This means that the techniques employed in the topology and architecture of the LDO, combined with the ones used in the layout design, allowed for a much more efficient use of die area.

Chapter 5

Simulations Results

The LDO layout design was extracted and simulated on the Cadence® Framework. The data was later processed on Matlab® for a better visualization. The post-layout simulations were divided into seven types of analyses:

- **Steady-State Response**: Covers the DC response of the LDO.
- **Stability**: Shows the open-loop frequency response of the LDO.
- **Power Supply Rejection Ratio**: Presents the input voltage spuria attenuation throughout the frequency spectrum.
- **Load Transient Response**: Illustrates the LDO response to sudden full range load current variations.
- **Load Regulation**: Quantifies the variation of the output voltage throughout the entire load current range.
- **Line Transient Response**: Depicts the LDO response to sudden full range input supply variations.
- **Line Regulation**: Quantifies the variation of the output voltage throughout the entire input supply range.

Moreover, each analysis comprises a set of simulations that characterizes the performance of the LDO. The simulations chosen were the following:

- **Nominal Performance**: Verifies the behavior of the LDO at normal conditions (ambient temperature of 27°C).
- **Temperature Sweep**: Revises the behavior of the LDO within the industrial temperature range (from -40°C to 85°C).
- **Monte Carlo Analysis**: Demonstrates the behavior of the LDO when experiencing random fabrication process imperfections (200 samples).

5.1 Steady-State Response

5.1.1 Nominal Performance

Figure 5.1 shows the quiescent current (I_Q) of the LDO throughout the entire load current (I_{LOAD}) range. As it can observed, it remains below 60 μA (spec given in Table 3.1) at all times and reaches its maximum value at full-load condition.

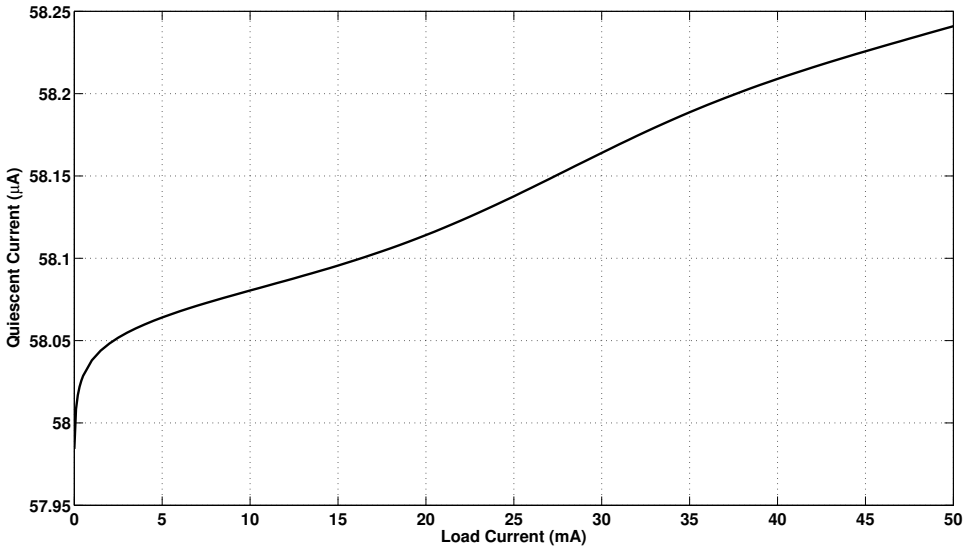


Figure 5.1: Quiescent current (I_Q).

Figures 5.2 and 5.3 illustrate the output power (P_{out}) and power efficiency (η) of the LDO, respectively, and they can be expressed as

$$\eta = \frac{P_{out}}{P_{TOT}} = \frac{V_{out} I_{LOAD}}{V_{supp}(I_Q + I_{LOAD})}. \tag{5.1}$$

Furthermore, η reaches its highest value at full-load condition as well, and remains above 80% all throughout the high and medium load condition (down to $I_{LOAD} = 500\ \mu A$). The performance summary is detailed in Table 5.1.

Table 5.1: Steady-state nominal performance summary.

$\mathbf{I_{Q_{max}}}$	58.241 μA
$\eta_{\mathbf{max}}$	89.79%
η @ **500** μ**A**	80.65%

The output voltage behavior dependent of the load current has not been shown here because the analysis will be performed more thoroughly on section 5.5. However, it has been included in the load current based DC analysis. The results are listed in Table 5.2.

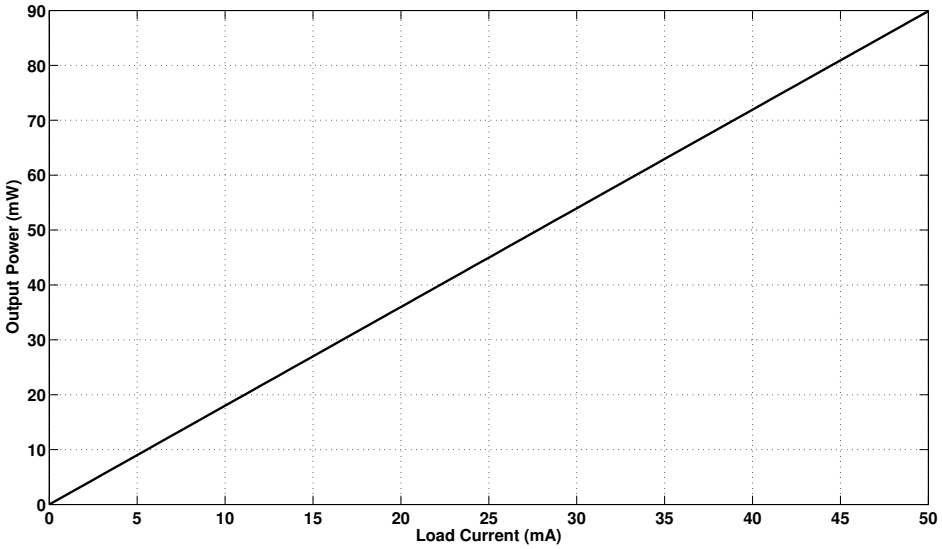


Figure 5.2: Output power (P_{out}).

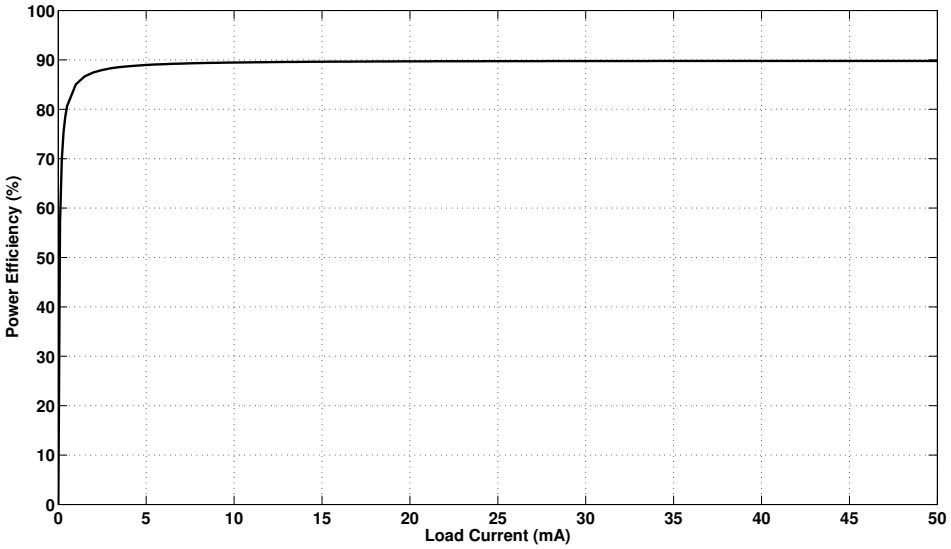


Figure 5.3: Power efficiency (η).

Table 5.2: Load current based DC nominal performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$	$\mathbf{I_{LOAD} = 5\ mA}$	$\mathbf{I_{LOAD} = 50\ mA}$
$\mathbf{I_Q}$ $(\mu\mathbf{A})$	58.008	58.064	58.241
$\mathbf{V_{out}}$ $(\mathbf{V})$	1.8003	1.8000	1.7979
$\mathbf{P_{out}}$ $(\mathbf{mW})$	0.00	9.00	89.89
η (%)	0.00	88.97	89.79

5.1.2 Temperature Sweep

Figure 5.4 illustrates the quiescent current (I_Q) curve shifts due to temperature variations. As it can observed, all curves remain below 60 μA (spec given in Table 3.1) throughout the entire temperature range. Moreover, the highest curve shift corresponds to the maximum temperature.

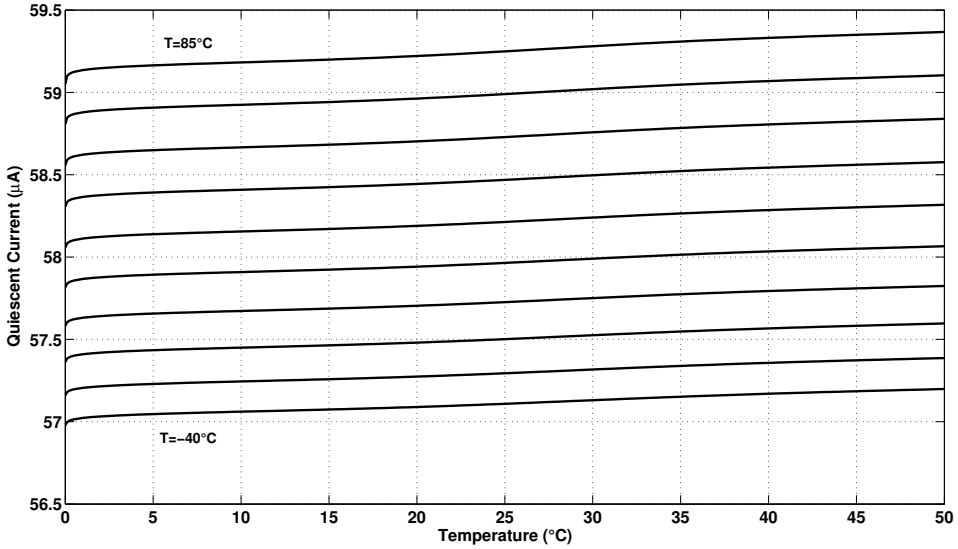


Figure 5.4: Temperature sweep of the quiescent current (I_Q).

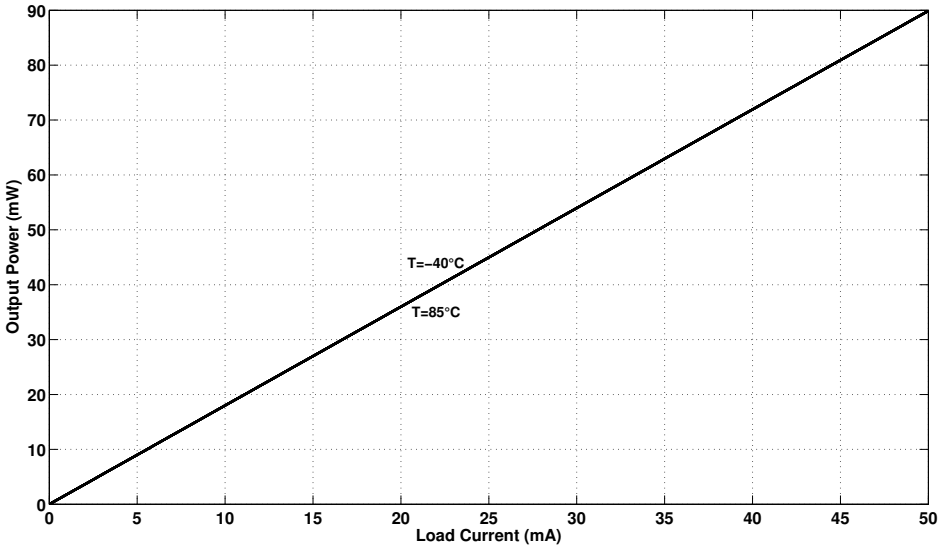


Figure 5.5: Temperature sweep of the output power (P_{out}).

Figures 5.5 and 5.6 illustrate the output power (P_{out}) and power efficiency (η) curve shifts caused by temperature variations, respectively. As it can be noticed,

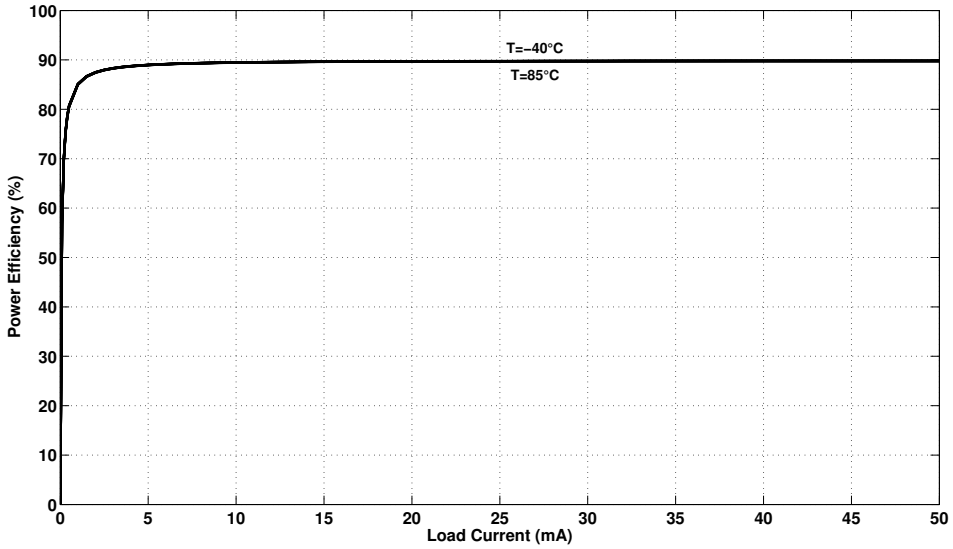


Figure 5.6: Temperature sweep of the power efficiency (η).

both parameters experience very small curve shifts and achieve the lowest one at the maximum temperature. Hence, a power efficiency above 80% down to the lower limit of the medium load condition (I_{LOAD} = 500 μA) is ensured throughout the entire temperature range, as it can be verified in Figure 5.7.

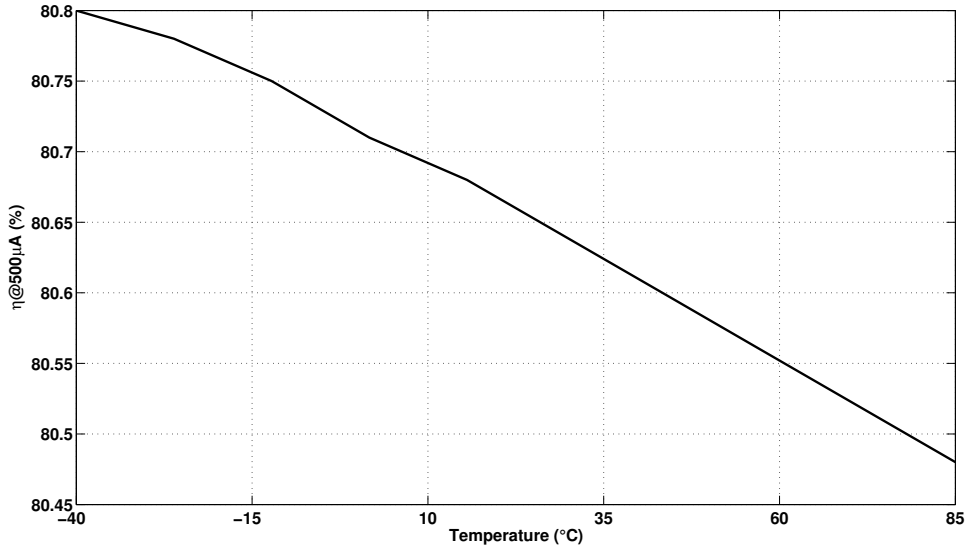


Figure 5.7: Temperature sweep of the η@500uA.

As expected, the worst case scenario occurs at the maximum temperature. The temperature sweep of the maximum quiescent current ($I_{Q_{max}}$) and maximum power efficiency (η_{max}) are not displayed here because they will be shown in the load

current based DC analysis for the heavy-load condition. The performance summary - expressed in temperature coefficients (TC) - is detailed Table 5.3.

Table 5.3: Steady-state temperature sweep performance summary.

$\mathbf{TC_{I_{Q_{max}}}}$	0.0173 $ppm/°C$
$\mathbf{TC_{\eta_{max}}}$	80.000 $ppm/°C$
$\mathbf{TC_{\eta@500\mu A}}$	2.560 ‰/$°C$

The temperature variations of the DC performance indicators for light-load ($I_{LOAD} = 0\ mA$), medium-load ($I_{LOAD} = 5\ mA$) and heavy-load ($I_{LOAD} = 50\ mA$) conditions are illustrated in Figures 5.8, 5.9 and 5.10, respectively.

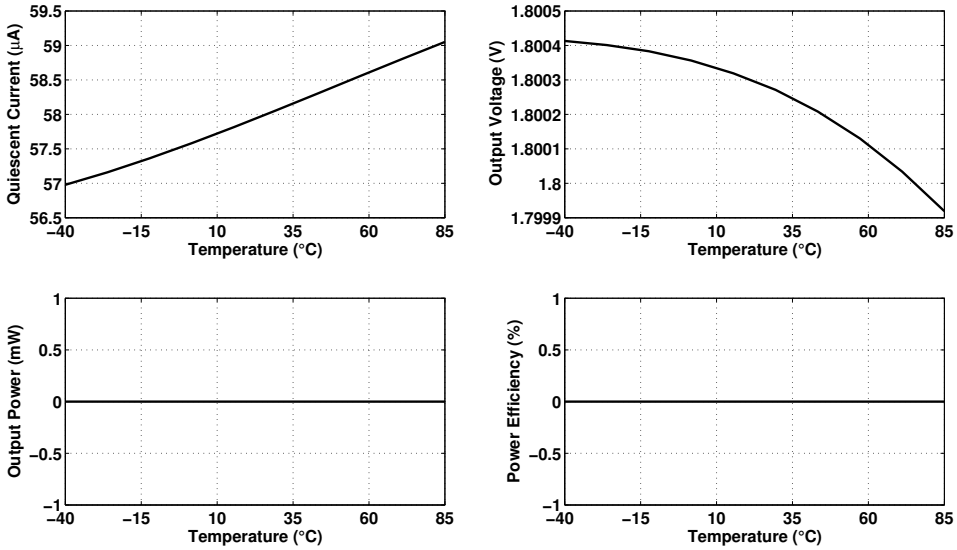


Figure 5.8: Temperature sweep of the quiescent current (top left corner), output voltage (top right corner), output power (bottom left corner), and power efficiency (bottom right corner) for $I_{LOAD} = 0\ mA$.

As it can be observed, I_Q and the η present a pretty linear behavior, whereas V_{out} and P_{out} do not. Furthermore, I_Q becomes more sensitive to temperature variations with high load currents. On the contrary, V_{out}, P_{out} and η become more sensitive with low load currents. The performance summary is displayed in Table 5.4.

Table 5.4: Load current based DC temperature sweep performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$	$\mathbf{I_{LOAD} = 5\ mA}$	$\mathbf{I_{LOAD} = 50\ mA}$
$\mathbf{TC_{I_Q}}$ $\mathbf{(ppm/°C)}$	0.0166	0.0169	0.0173
$\mathbf{TC_{V_{out}}}$ $\mathbf{(ppm/°C)}$	3.952	4.088	0.336
$\mathbf{TC_{P_{out}}}$ $\mathbf{(ppm/°C)}$	-	0.020	0.017
$\mathbf{TC_{\eta}}$ (‰/$\mathbf{°C}$)	-	0.500	0.048

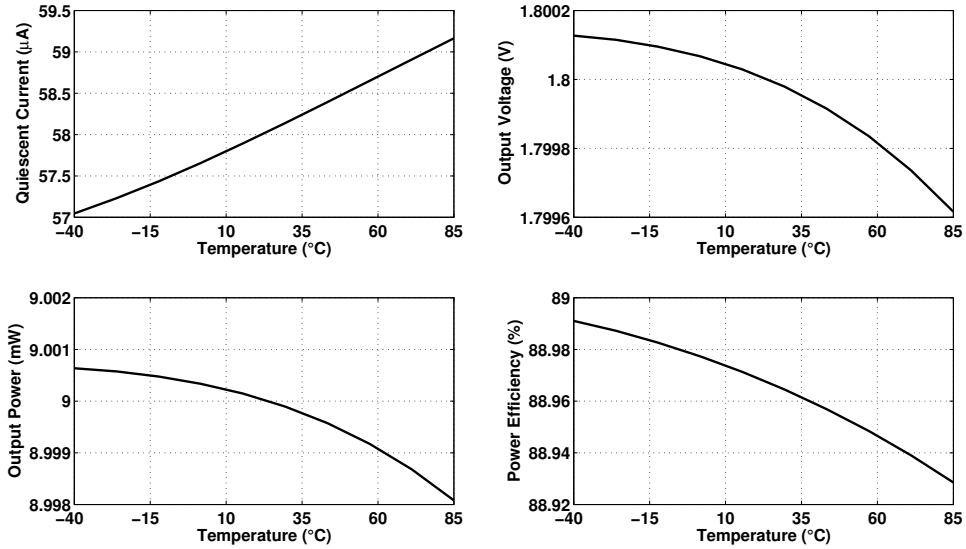


Figure 5.9: Temperature sweep of the quiescent current (top left corner), output voltage (top right corner), output power (bottom left corner), and power efficiency (bottom right corner) for $I_{LOAD} = 5\ mA$.

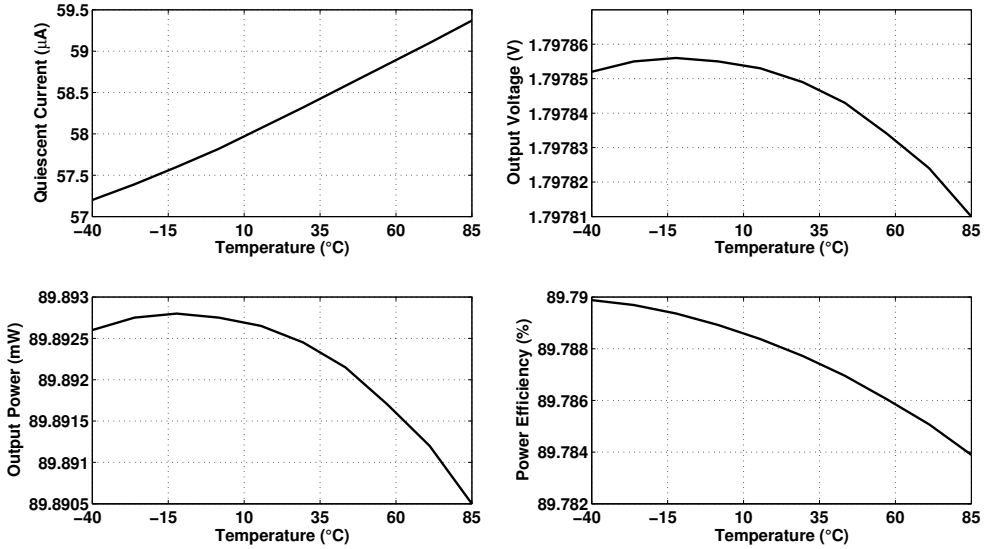


Figure 5.10: Temperature sweep of the quiescent current (top left corner), output voltage (top right corner), output power (bottom left corner), and power efficiency (bottom right corner) for $I_{LOAD} = 50\ mA$.

5.1.3 Monte Carlo Analysis

Figure 5.11 illustrates the monte carlo analysis of the quiescent current (I_Q). Though there is one sample that moves further away from the mean performance, all samples remain below 60 μA (spec given in Table 3.1).

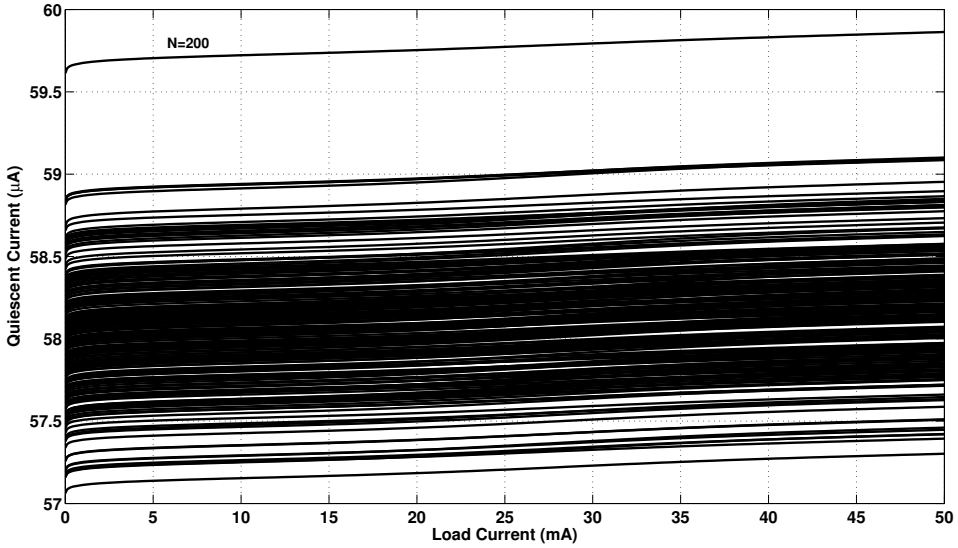


Figure 5.11: Monte carlo analysis of the quiescent current (I_Q).

Figures 5.12 and 5.13 show the monte carlo analysis of the output power (P_{out}) and power efficiency (η), respectively.

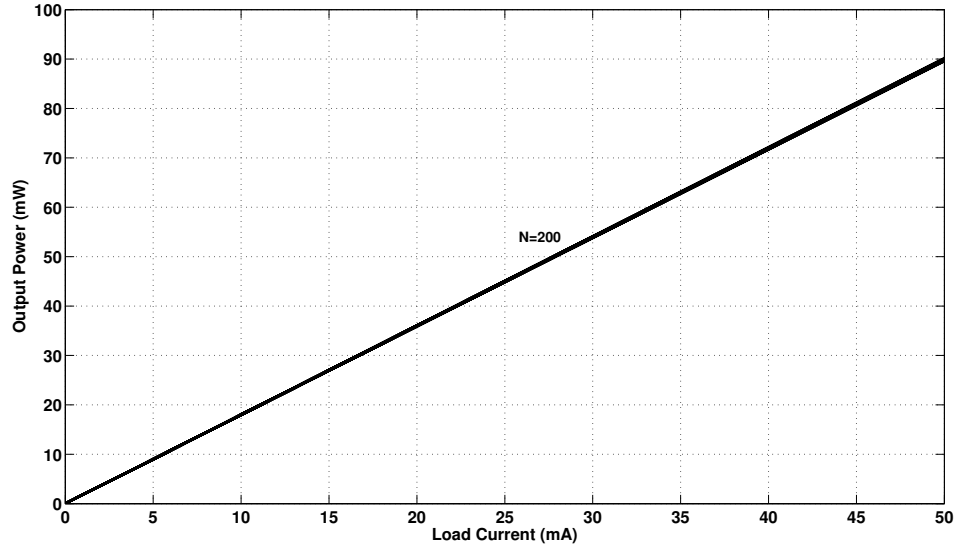


Figure 5.12: Monte carlo analysis of the output power (P_{out}).

As it can be noticed, both parameters are highly resilient to process variables variations and mismatch effects. Hence, a power efficiency above 80% down to the lower limit of the medium load condition ($I_{LOAD} = 500\ \mu A$) is ensured, as it can be verified in Figure 5.14. The monte carlo analysis a of the maximum quiescent current ($I_{Q_{max}}$) and maximum power efficiency (η_{max}) are not displayed here because they

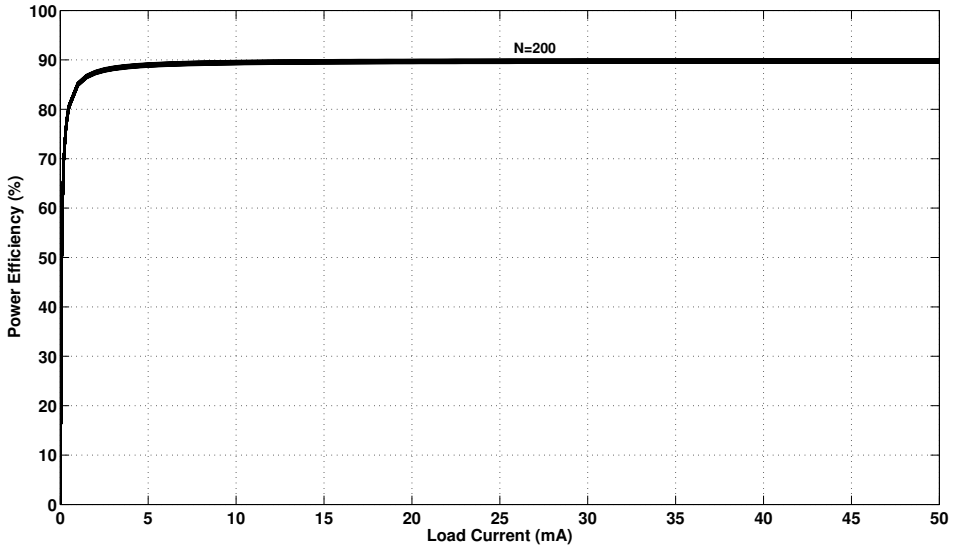


Figure 5.13: Monte carlo analysis of the power efficiency (η).

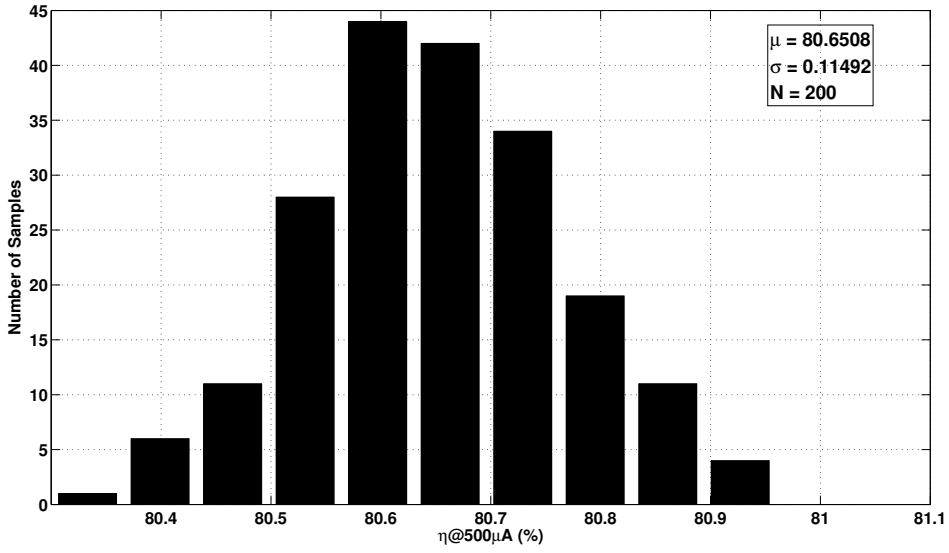


Figure 5.14: Monte carlo analysis of the η@500uA.

will be shown in the load current based DC analysis for the heavy-load condition. The performance summary - described by the mean (μ) and standard deviation (σ) - is detailed Table 5.5.

Table 5.5: Steady-state monte carlo analysis performance summary.

$\mathbf{I_{Q_{max}}}$	$\mu = 58.21\ \mu A$	$\sigma = 0.38\ \mu A$
$\eta_{\mathbf{max}}$	$\mu = 89.78\%$	$\sigma = 0.12\%$
η@$\mathbf{500}\mu\mathbf{A}$	$\mu = 80.65\%$	$\sigma = 0.11\%$

The monte carlo analyses of the DC performance indicators for light-load ($I_{LOAD} = 0\ mA$), medium-load ($I_{LOAD} = 5\ mA$) and heavy-load ($I_{LOAD} = 50\ mA$) conditions are illustrated in Figures 5.15, 5.16 and 5.17, respectively.

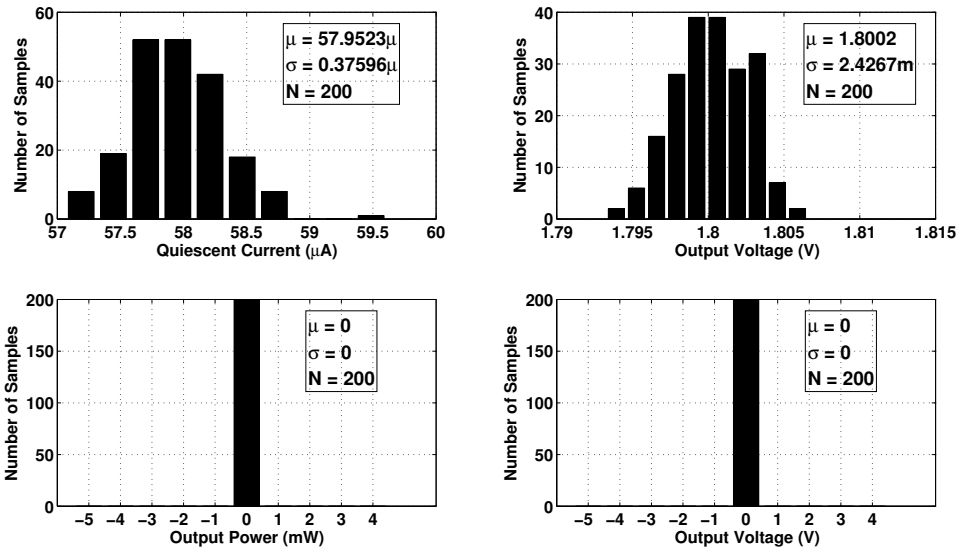


Figure 5.15: Monte carlo analysis of the quiescent current (top left corner), output voltage (top right corner), output power (bottom left corner), and power efficiency (bottom right corner) for $I_{LOAD} = 0\ mA$.

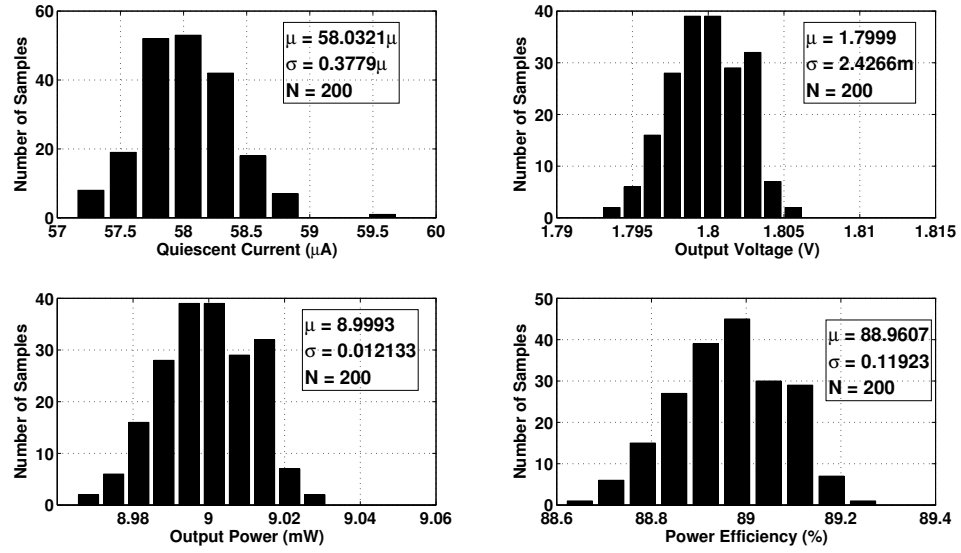


Figure 5.16: Monte carlo analysis of the quiescent current (top left corner), output voltage (top right corner), output power (bottom left corner), and power efficiency (bottom right corner) for $I_{LOAD} = 5\ mA$.

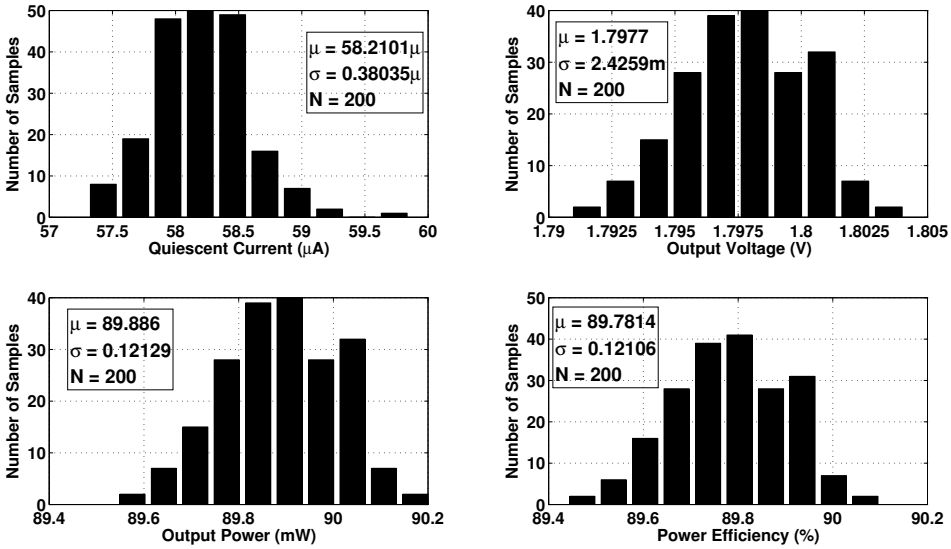


Figure 5.17: Monte carlo analysis of the quiescent current (top left corner), output voltage (top right corner), output power (bottom left corner), and power efficiency (bottom right corner) for $I_{LOAD} = 50\ mA$.

As it can be observed, the output voltage becomes slightly more sensitive to fabrication process imperfections with low load currents, whereas the quiescent current experiences the opposite effect. The performance summary is detailed in Table 5.6

Table 5.6: Load current based DC monte carlo performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$		$\mathbf{I_{LOAD} = 5\ mA}$		$\mathbf{I_{LOAD} = 50\ mA}$	
	μ	σ	μ	σ	μ	σ
$\mathbf{I_Q}$ $(\mu\mathbf{A})$	57.952	0.376	58.032	0.378	58.210	0.380
$\mathbf{V_{out}}$ $(\mathbf{V})$	1.8002	$2.4267m$	1.7999	$2.4266m$	1.7977	$2.4259m$
$\mathbf{P_{out}}$ $(\mathbf{mW})$	-		8.999	0.012	89.886	0.121
η (%)	-		88.96	0.119	89.78	0.121

5.2 Stability

5.2.1 Nominal Performance

The open-loop response of the LDO for all three load current conditions is depicted in Figure 5.18. A zoomed-in view around the UGF of the three curves is captioned in Figure 5.19 for a better visualization.

A PM above 60° is achieved in all scenarios. The phase curve for the full-load condition starts at 0° instead of 180°. This phenomenon occurs due to the operation of the adaptive active feedback block, which was simplified in the small-

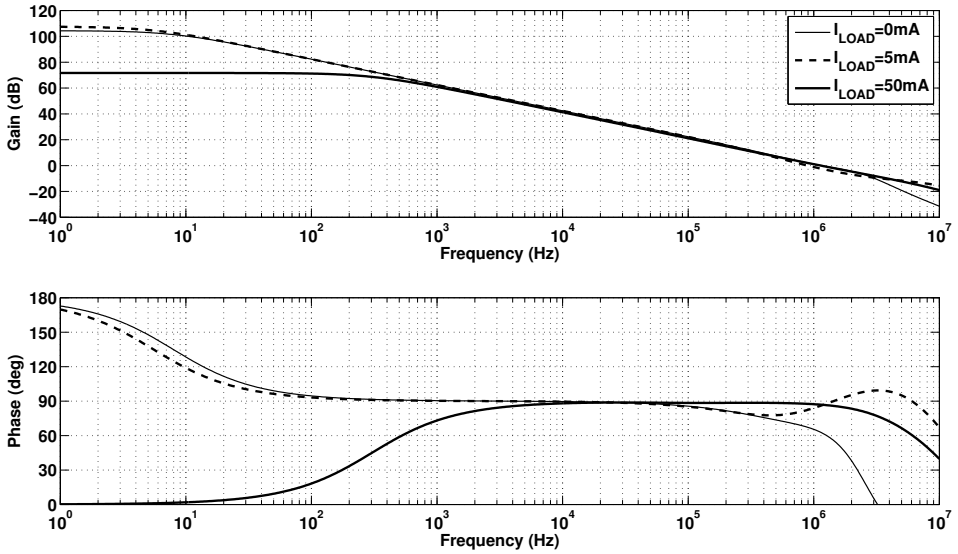


Figure 5.18: Open-loop response for different load currents (I_{LOAD}).

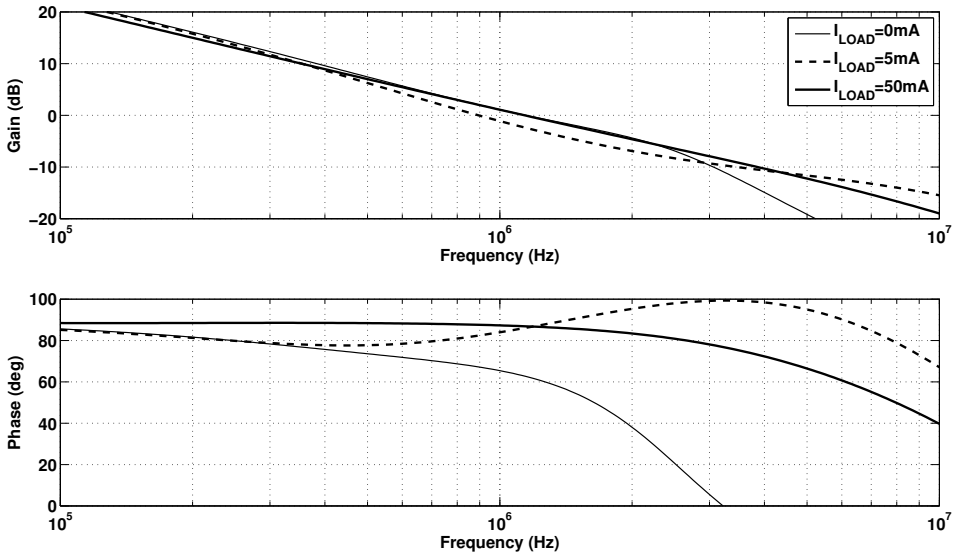


Figure 5.19: Zoomed-in view of the open-loop response for different load currents.

signal analysis. However, this is just an interpretation of the simulator and has no effect on the analysis end result. The stability performance summary is described in Table 5.7.

Table 5.7: Stability performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$	$\mathbf{I_{LOAD} = 5\ mA}$	$\mathbf{I_{LOAD} = 50\ mA}$
PM (°)	62.63	82.36	86.88
UGF (**MHz**)	1.146	0.894	1.138

5.2.2 Temperature Sweep

The temperature sweeps of the open-loop responses of the LDO for light-load ($I_{LOAD} = 0\ mA$), medium-load ($I_{LOAD} = 5\ mA$) and heavy-load ($I_{LOAD} = 50\ mA$) conditions are depicted in Figures 5.20, 5.22 and 5.24, respectively. A zoomed-in view around the UGF of the open-loop response at each scenario is captioned in Figures 5.21, 5.23 and 5.25, respectively.

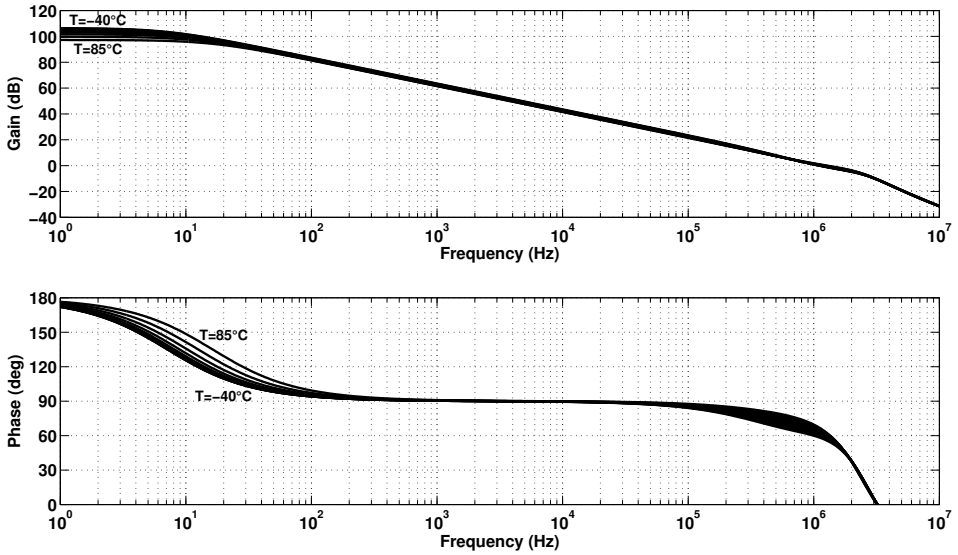


Figure 5.20: Temperature sweep of the open-loop response for $I_{LOAD} = 0\ mA$.

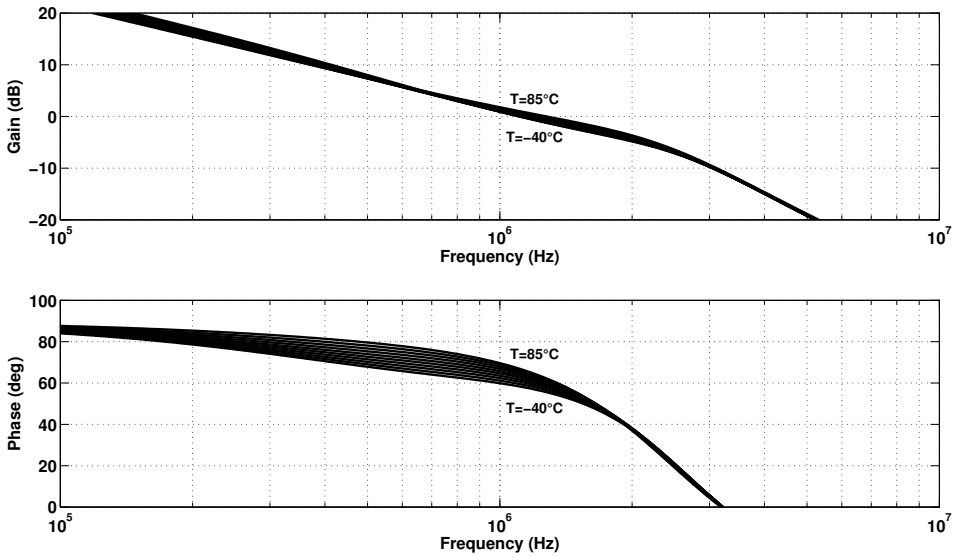


Figure 5.21: Zoomed-in view of the temperature sweep of the open-loop response for $I_{LOAD} = 0\ mA$.

At the light-load condition case, the temperature increment causes the DC OLG to diminish and the UGF to augment. The variation is quite small nonetheless.

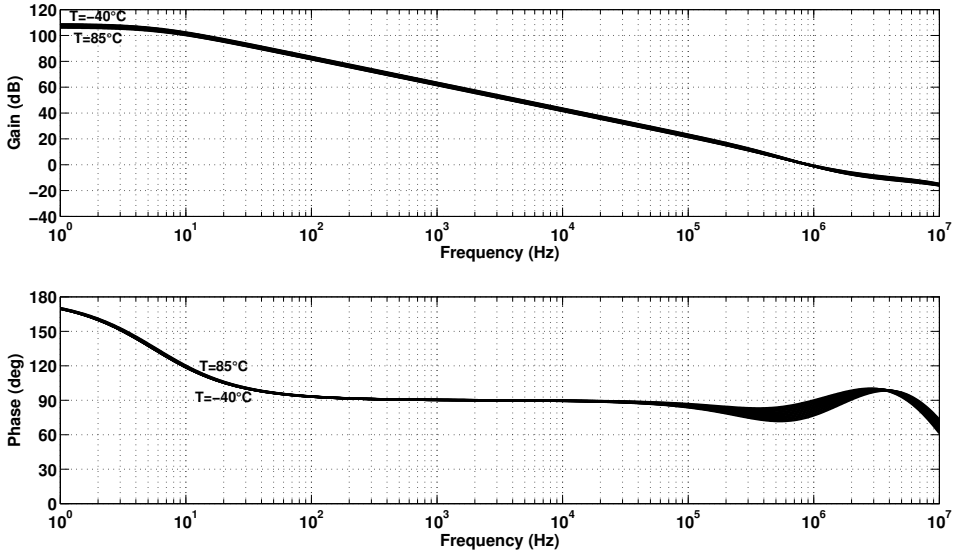


Figure 5.22: Temperature sweep of the open-loop response for $I_{LOAD} = 5\ mA$.

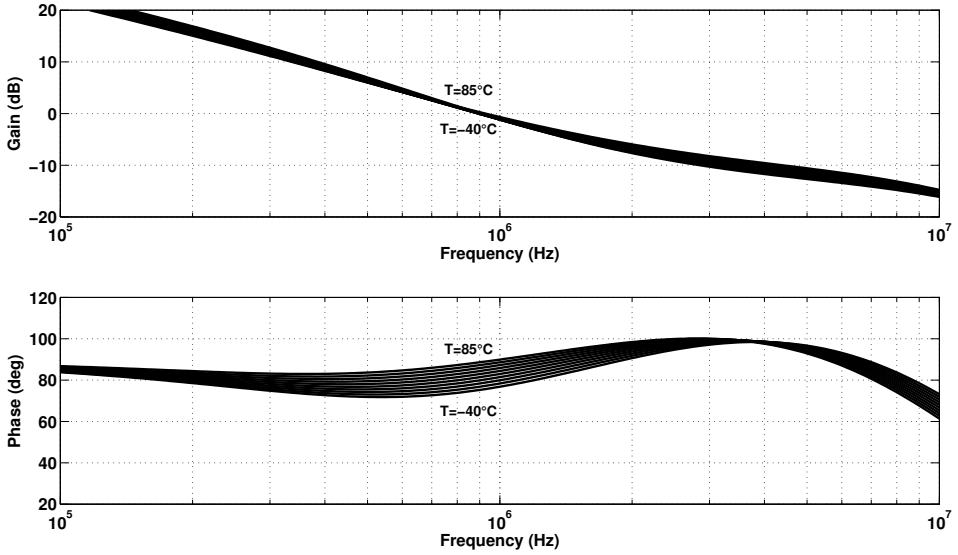


Figure 5.23: Zoomed-in view of the temperature sweep of the open-loop response for $I_{LOAD} = 5\ mA$.

At the medium-load condition, the temperature has the same effect. However, the DC OLG abatement is even smaller and the UGF increment is slightly higher compared to the light-load condition.

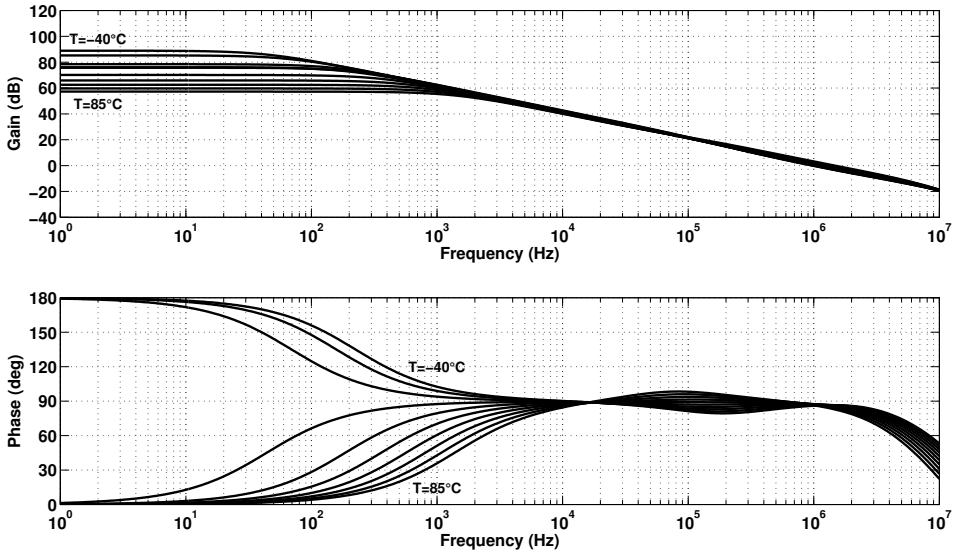


Figure 5.24: Temperature sweep of the open-loop response for $I_{LOAD} = 50\ mA$.

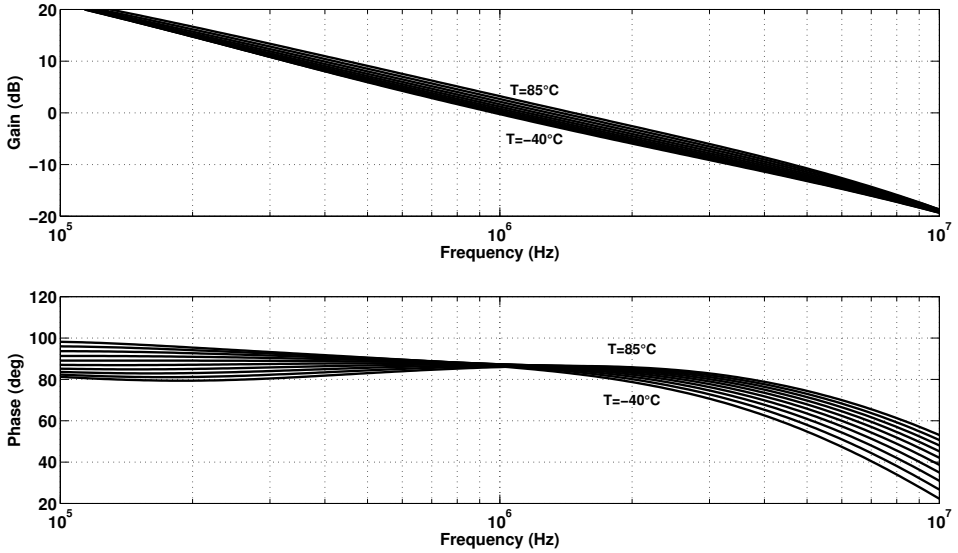


Figure 5.25: Zoomed-in view of the temperature sweep of the open-loop response for $I_{LOAD} = 50\ mA$.

Finally, the heavy-load condition is no exception to the other two. Nevertheless, the LDO is far more sensitive with high current loads. The variation of the DC OLG and the UGF in this scenario highly surpasses the one in the other two. Additionally, the phase DC value fluctuates between 0° and 180°, which implicates that the adaptive active feedback is the more sensitive subunit of the LDO. Thus, the more "activated" the block (heavy-load condition), the higher the temperature sensitivity of the frequency response.

The temperature dependent variation of the stability performance indicators (PM and UGF) for light, medium, and heavy-load condition are portraited in Figures 5.26, 5.27 and 5.28, respectively.

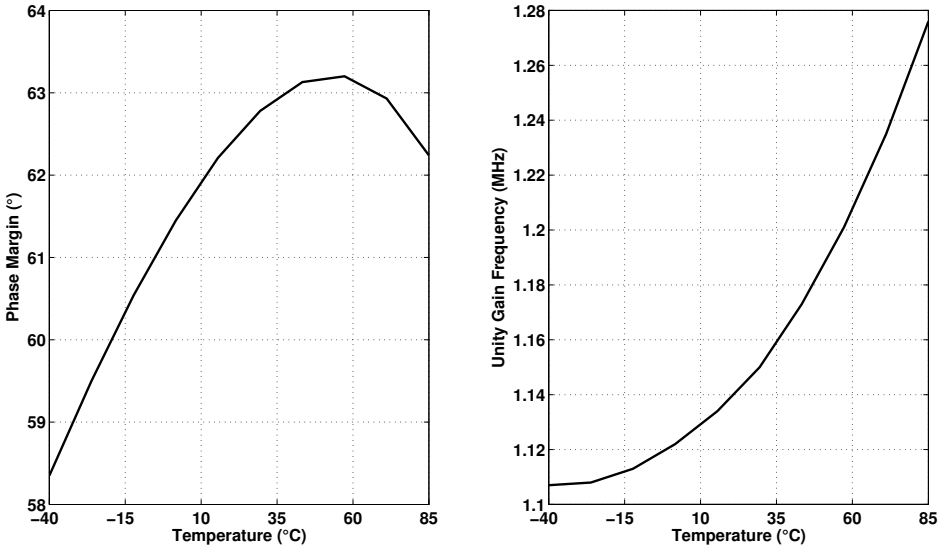


Figure 5.26: Temperature sweep of the phase margin (left) and unity gain frequency (right) for $I_{LOAD} = 0\ mA$.

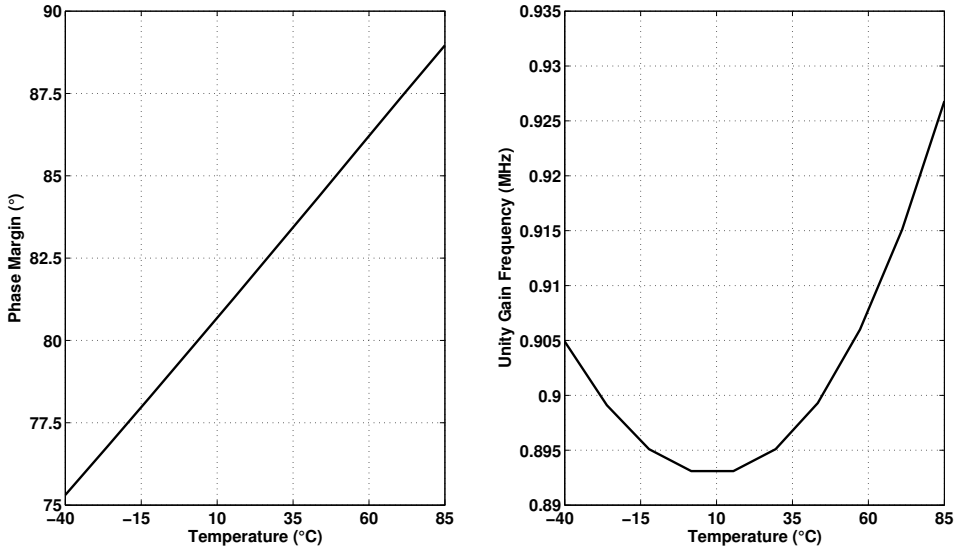


Figure 5.27: Temperature sweep of the phase margin (left) and unity gain frequency (right) for $I_{LOAD} = 5\ mA$.

As it can be visualized, most of them do not present a linear behavior or follow any pattern. The PM worst case scenario occurs at the light-load condition at

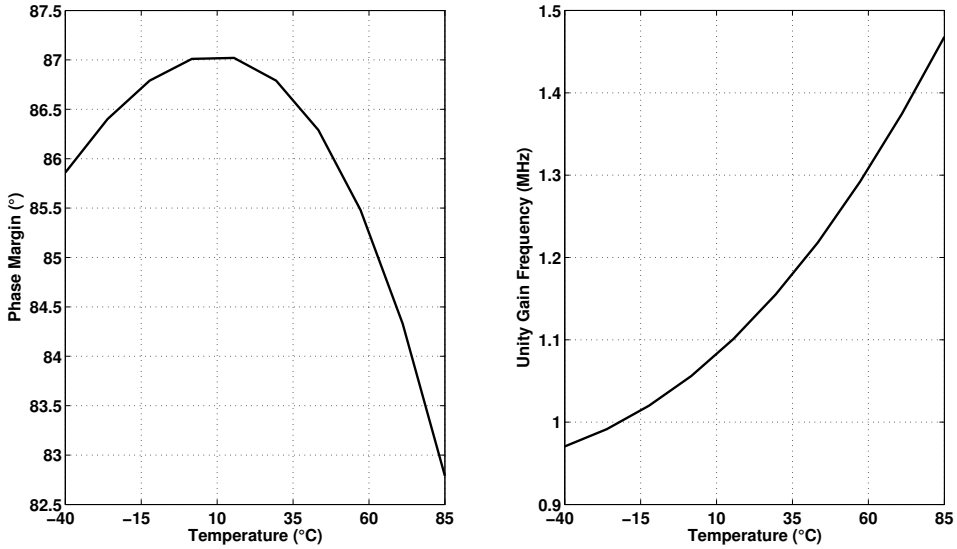


Figure 5.28: Temperature sweep of the phase margin (left) and unity gain frequency (right) for $I_{LOAD} = 50\ mA$.

temperatures below -15°C, where it becomes lower than 60°. Nevertheless, the real constraint, stability-wise, is 45°. Therefore, it can be stated that the LDO remains highly stable. On the other hand, the UGF worst scenario takes place at heavy-load condition at temperatures below -15°C as well, where it falls behind 1 MHz. This is considered the worst case because a high loop-bandwidth is most needed with high load-currents to ensure a fast transient response. However, the fast transient response of the LDO is mainly provided by the SRE. Moreover, the UGF in this scenario remains fairly close to 1 MHz. On that account, it can be stated that the speed of the LDO is not really compromised. The stability performance summary is displayed in Table 5.8.

Table 5.8: Stability temperature sweep performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$	$\mathbf{I_{LOAD} = 5\ mA}$	$\mathbf{I_{LOAD} = 50\ mA}$
$\mathbf{TC_{PM}}$ (‰/°C)	38.80	109.20	33.84
$\mathbf{TC_{UGF}}$ (kHz/°C)	1.352	0.270	3.980

5.2.3 Monte Carlo Analysis

The monte carlo analyses of the open-loop responses of the LDO for light-load ($I_{LOAD} = 0\ mA$), medium-load ($I_{LOAD} = 5\ mA$) and heavy-load ($I_{LOAD} = 50\ mA$) conditions are depicted in Figures 5.29, 5.31 and 5.33, respectively. A zoomed-in view around the UGF of the open-loop response at each scenario is captioned in Figures 5.30, 5.32 and 5.34, respectively.

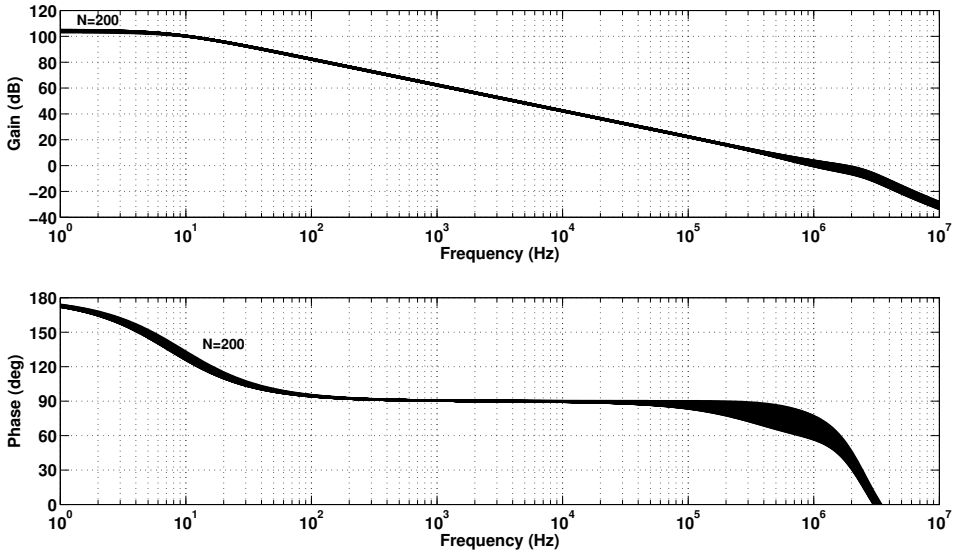


Figure 5.29: Monte carlo analysis of the open-loop response for $I_{LOAD} = 0\ mA$.

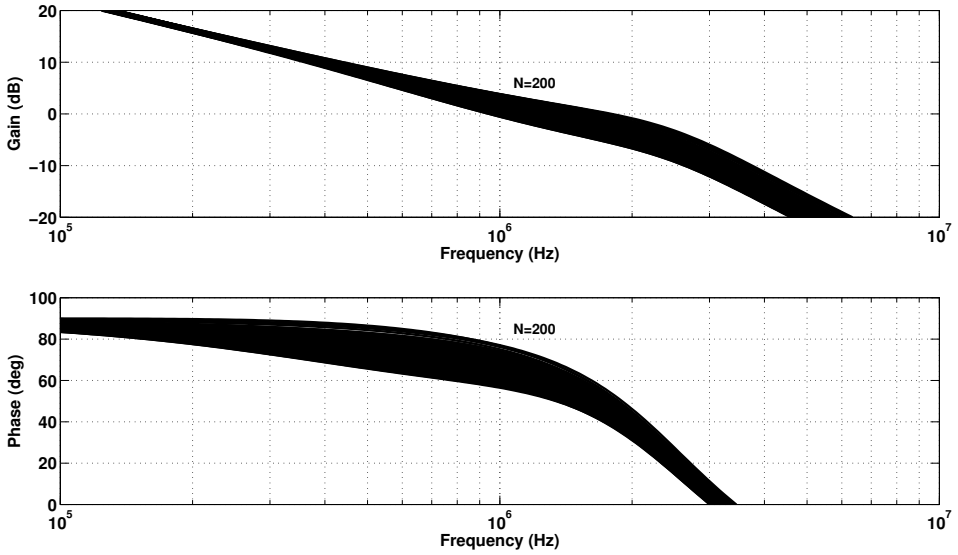


Figure 5.30: Zoomed-in view of the montecarlo analysis of the open-loop response for $I_{LOAD} = 0\ mA$.

At the light-load condition case, the LDO presents a high resilience towards process parameters variations and mismatch effects. The DC OLG is barely affected. Nevertheless, at frequencies close to the UGF the sensitivity rises, which may cause an increment in the PM and UGF variation range. Since the no-load condition is the most exigent one in terms of stability, the PM variation due to fabrication process imperfections at this scenario should be watched meticulously.

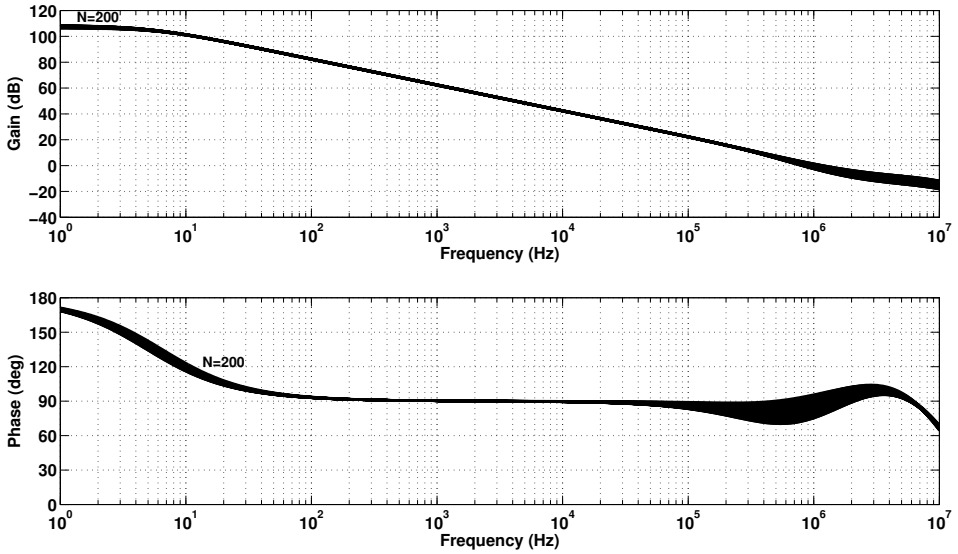


Figure 5.31: Monte carlo analysis of the open-loop response for $I_{LOAD} = 5\ mA$.

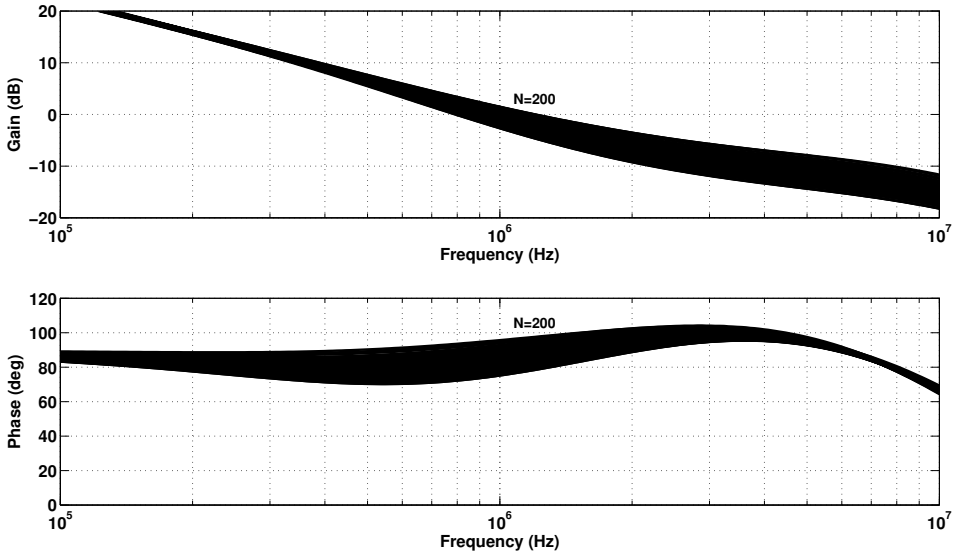


Figure 5.32: Zoomed-in view of the montecarlo analysis of the open-loop response for $I_{LOAD} = 5\ mA$.

At the medium-load condition case, the LDO presents a high resilience towards process parameters variations and mismatch effects as well. The DC OLG remains close to its nominal value. However, once again at frequencies close to the UGF the sensitivity increases, which may lead to an increment in the PM and UGF variation range.

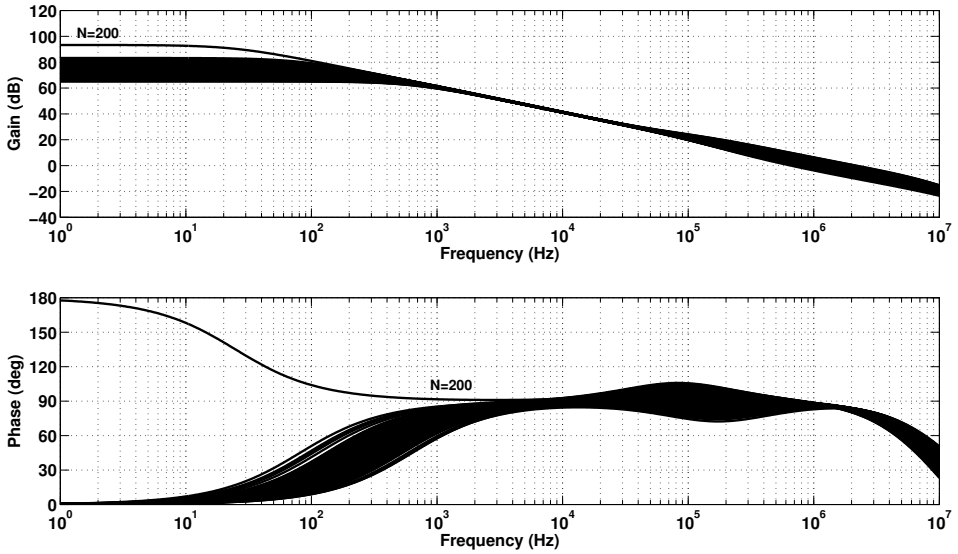


Figure 5.33: Monte carlo analysis of the open-loop response for $I_{LOAD} = 50\ mA$.

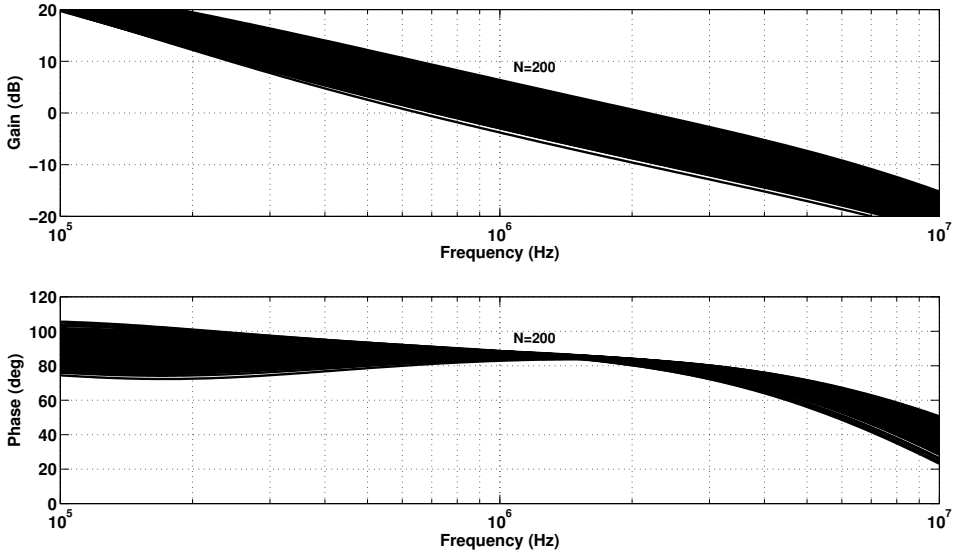


Figure 5.34: Zoomed-in view of the montecarlo analysis of the open-loop response for $I_{LOAD} = 50\ mA$.

At the heavy-load condition case, the LDO appears to be considerably more sensitive to process parameters variations and mismatch effects than for the other two cases. The DC OLG presents a high variation range (around 20 dB). Additionally, the phase DC value fluctuates between 0° and 180° and the pole-zero cancellation experiences significant changes, which thereby implies that the adaptive active feedback block is highly sensitive to fabrication process imperfections when driving high load currents.

The monte carlo analysis of the stability performance indicators (PM and UGF) for light, medium, and heavy-load condition are portraited in Figures 5.35, 5.36 and 5.37, respectively.

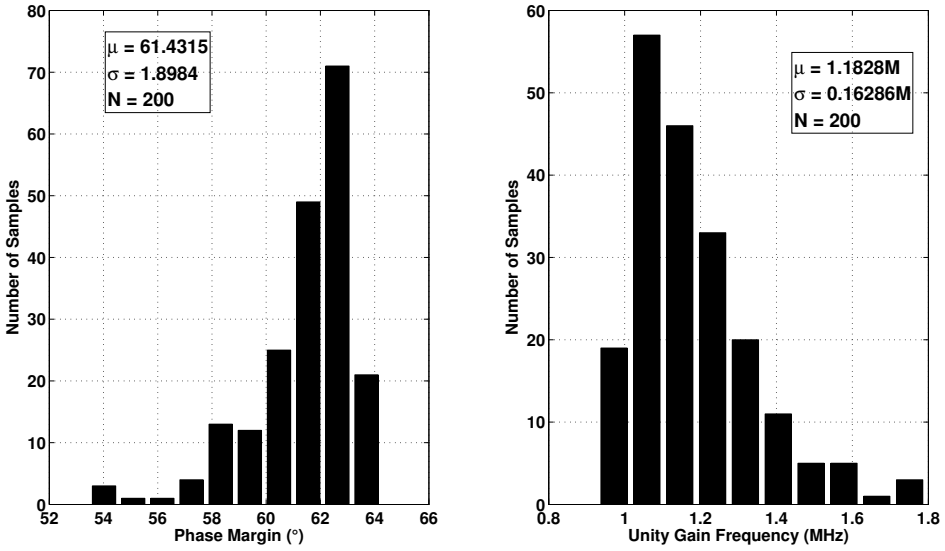


Figure 5.35: Monte carlo analysis of the phase margin (left) and unity gain frequency (right) for $I_{LOAD} = 0\ mA$.

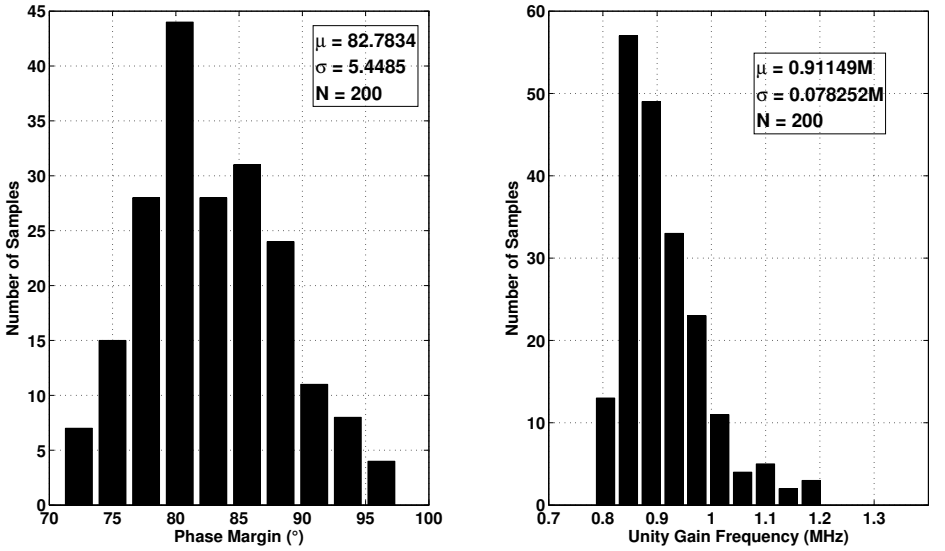


Figure 5.36: Monte carlo analysis of the phase margin (left) and unity gain frequency (right) for $I_{LOAD} = 5\ mA$.

As it can be observed, the medium-load condition presents the highest PM variation. Nevertheless, since in this scenario the LDO is highly stable, the operation of the

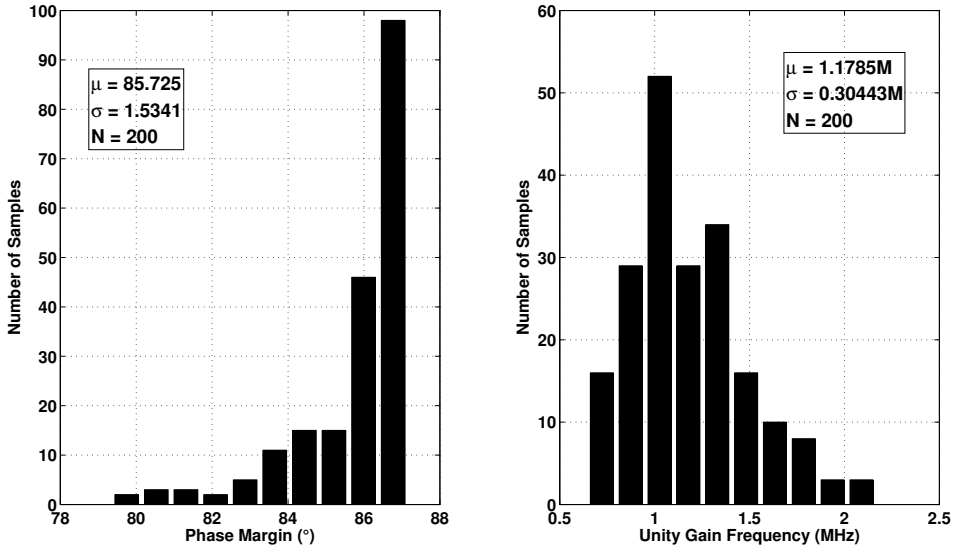


Figure 5.37: Monte carlo analysis of the phase margin (left) and unity gain frequency (right) for $I_{LOAD} = 50\ mA$.

circuit is not affected. That been said, at the no-load condition the PM does fall below 60°, which might be problematic. However, it remains considerably superior to 45°, which ensures stability. On the other hand, the UGF appears to be more sensitive at the heavy-load condition. A low UGF at this scenario implies a slow LDO. Nevertheless, since the SRE is in charge of compensating the main loop speed shortcomings, the situation is not critical. The performance summary is displayed in Table 5.9.

Table 5.9: Stability monte carlo analysis performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$		$\mathbf{I_{LOAD} = 5\ mA}$		$\mathbf{I_{LOAD} = 50\ mA}$	
	μ	σ	μ	σ	μ	σ
PM (°)	61.432	1.898	82.783	5.449	85.725	1.534
UGF (MHz)	1.183	0.163	0.911	0.078	1.179	0.304

5.3 Power Supply Rejection Ratio

5.3.1 Nominal Performance

Figure 5.38 illustrates the PSRR of the LDO for all three load current conditions. A zoomed-in view around 10 kHz is captioned in Figure 5.39 in order to verify the spec given in Table 3.1.

The no-load condition and medium-load condition ($I_{LOAD} = 5\ mA$) curves follow the same pattern up until the UGF of the LDO. Moreover, a PSRR below -40 dB

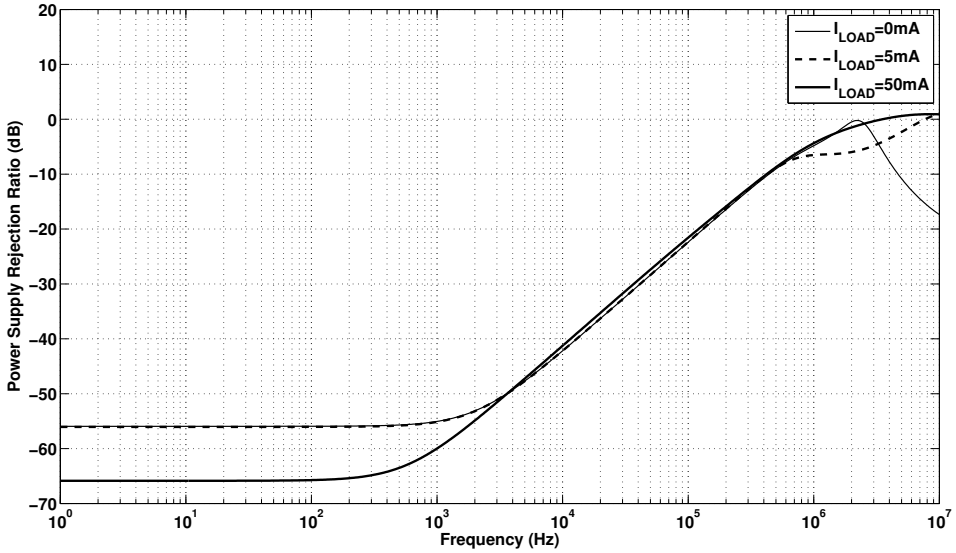


Figure 5.38: PSRR for different load currents (I_{LOAD}).

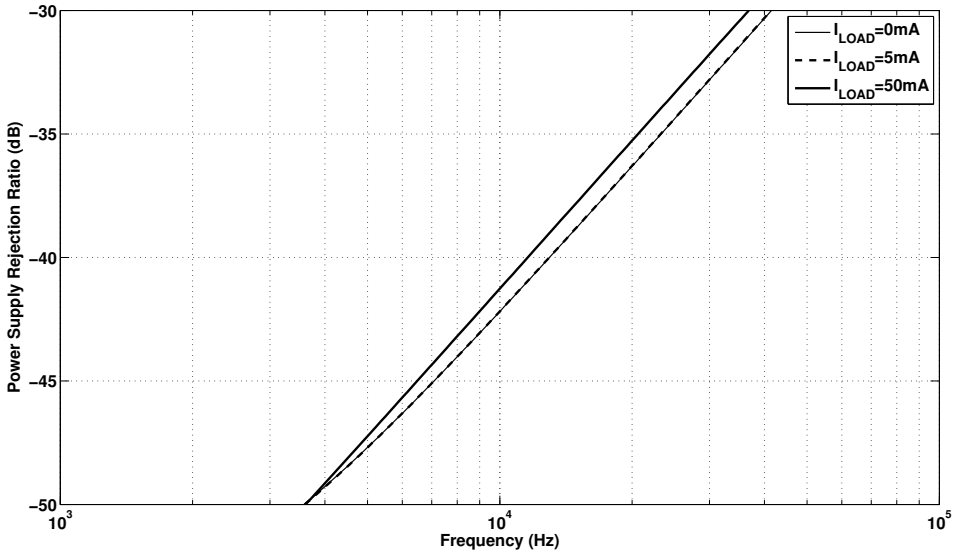


Figure 5.39: Zoomed-in view of the PSRR for different load currents (I_{LOAD}).

is attained at all load current scenarios. The actual values of the PSRR at the aforementioned frequency for all three load current conditions are detailed in Table 5.10.

Table 5.10: PSRR nominal performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$	$\mathbf{I_{LOAD} = 5\ mA}$	$\mathbf{I_{LOAD} = 50\ mA}$
PSRR@10kHz (dB)	-42.19	-42.18	-41.21

5.3.2 Temperature Sweep

The temperature sweeps of the PSRR for light-load ($I_{LOAD} = 0\ mA$), medium-load ($I_{LOAD} = 5\ mA$) and heavy-load ($I_{LOAD} = 50\ mA$) conditions is depicted in Figures 5.40, 5.42 and 5.44, respectively. A zoomed-in view around around 10 kHz at each scenario is captioned in Figures 5.41, 5.43 and 5.45, respectively.

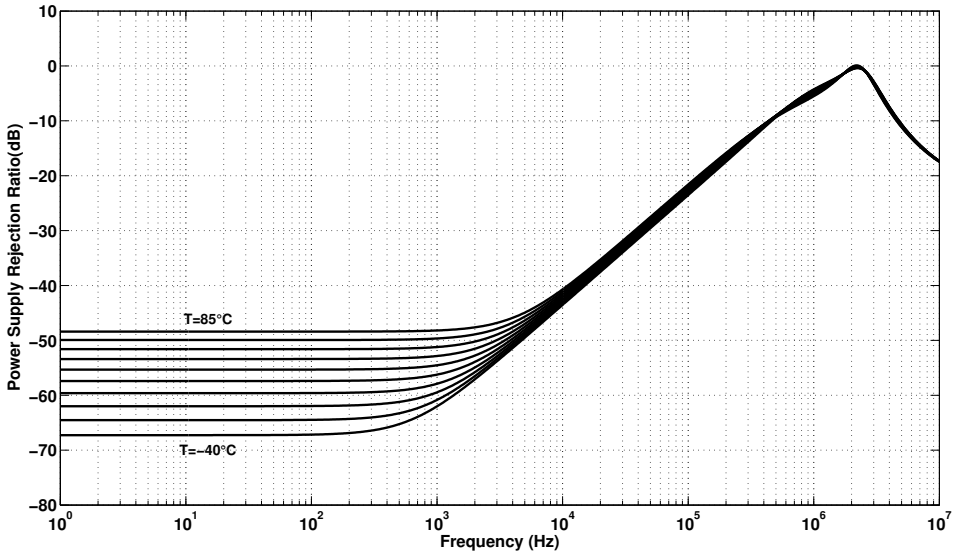


Figure 5.40: Temperature sweep of the PSRR for $I_{LOAD} = 0\ mA$.

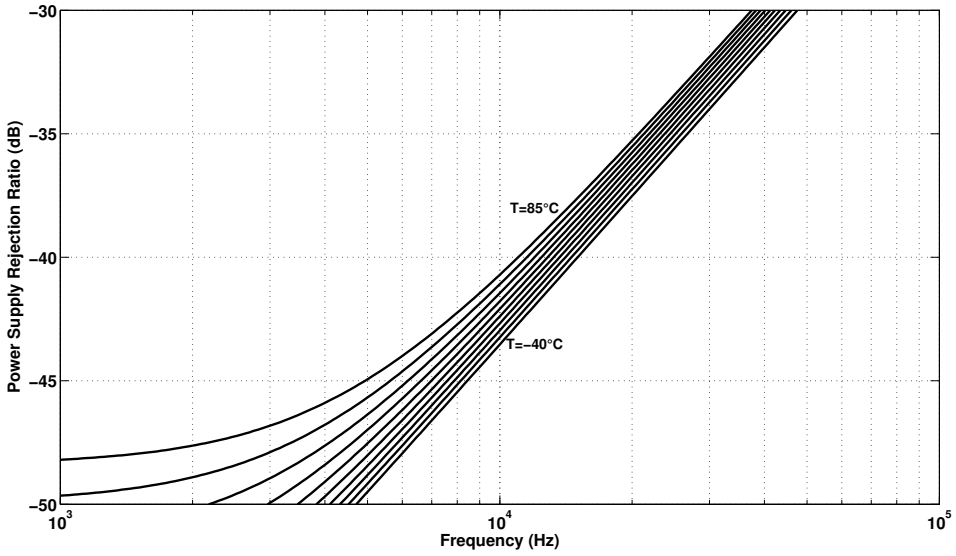


Figure 5.41: Zoomed-in view of the temperature sweep of the PSRR for $I_{LOAD} = 0\ mA$.

At the light-load condition, the DC PSRR magnitude decreases as the temperature increases. At this range (low frequencies), the curve shifts are quite significant.

However, once the dominant pole of the system is surpassed, the curve shifts start to become much smaller at a high pace. Consequently, all PSRR curves meet the specification given in Table 3.1.

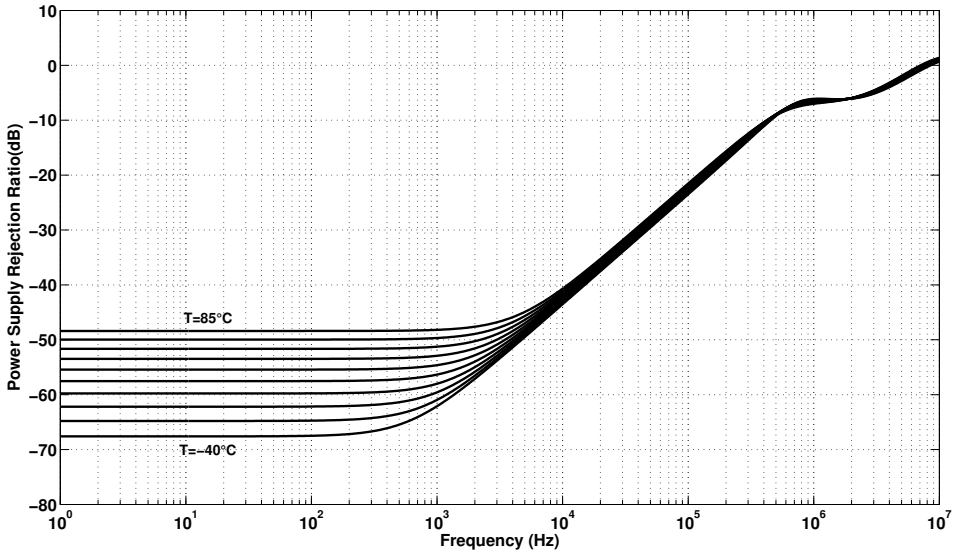


Figure 5.42: Temperature sweep of the PSRR for $I_{LOAD} = 5\ mA$.

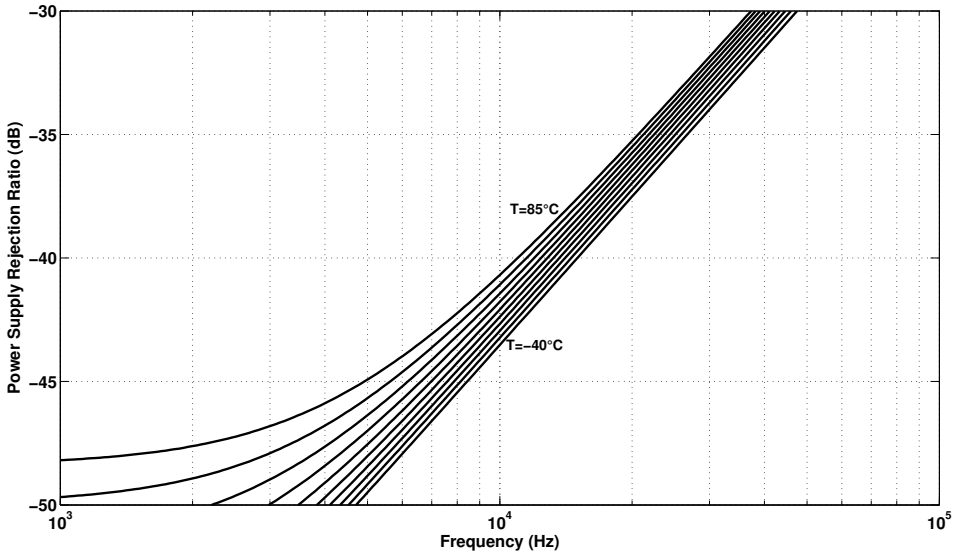


Figure 5.43: Zoomed-in view of the temperature sweep of the PSRR for $I_{LOAD} = 5\ mA$.

At the medium-load condition, the PSRR curves follow a very similar pattern as the light-load condition ones. As a result, all PSRR curves meet the specification given in Table 3.1.

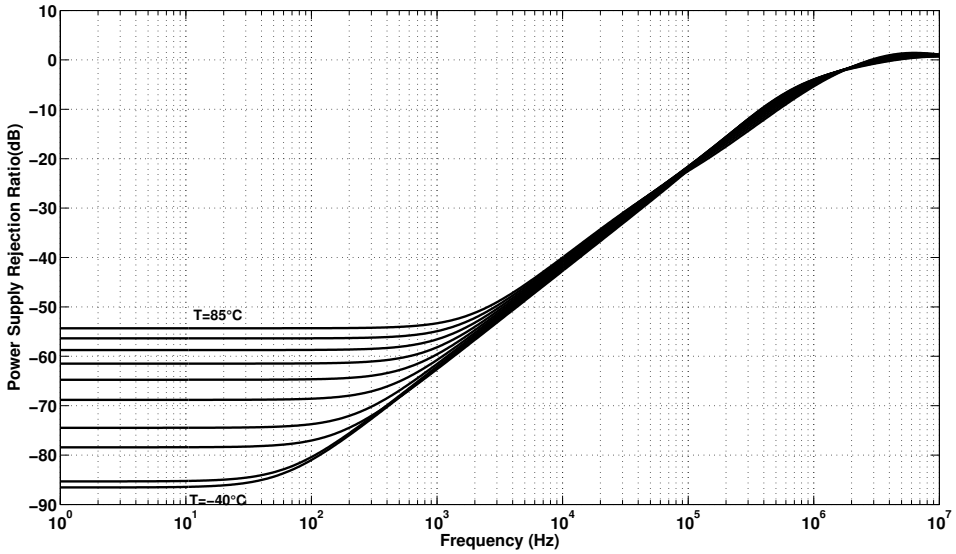


Figure 5.44: Temperature sweep of the PSRR for $I_{LOAD} = 50\ mA$.

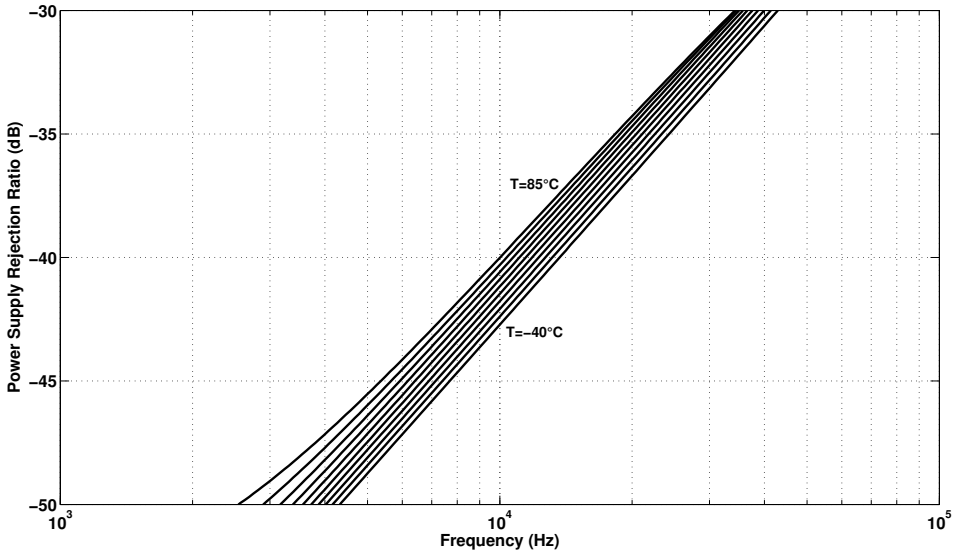


Figure 5.45: Zoomed-in view of the temperature sweep of the PSRR for $I_{LOAD} = 50\ mA$.

At the heavy-load condition, the DC PSRR magnitude decreases as the temperature increases once more. However, at these range (low frequencies), the curve shifts are much larger than for the other two cases. Nonetheless, once the dominant pole of the system is surpassed, the curve shifts start to become much smaller, as it did for the other two scenarios. As a consequence, though the PSRR curves get much closer to the limit, they all meet the specification given in Table 3.1.

The temperature sweep of the PSRR at the 10 kHz frequency for light-load, medium-load, and heavy-load conditions is illustrated in Figures 5.46, 5.47 and 5.48. As it can be observed, they all present a standard liner behavior. The worst case scenario takes places at the heavy-load condition at the maximum temperature. Nevertheless, the PSRR remains below -40 dB even at this scenario. The temperature coefficient of the PSRR at this frequency for each load condition is listed in Table 5.11.

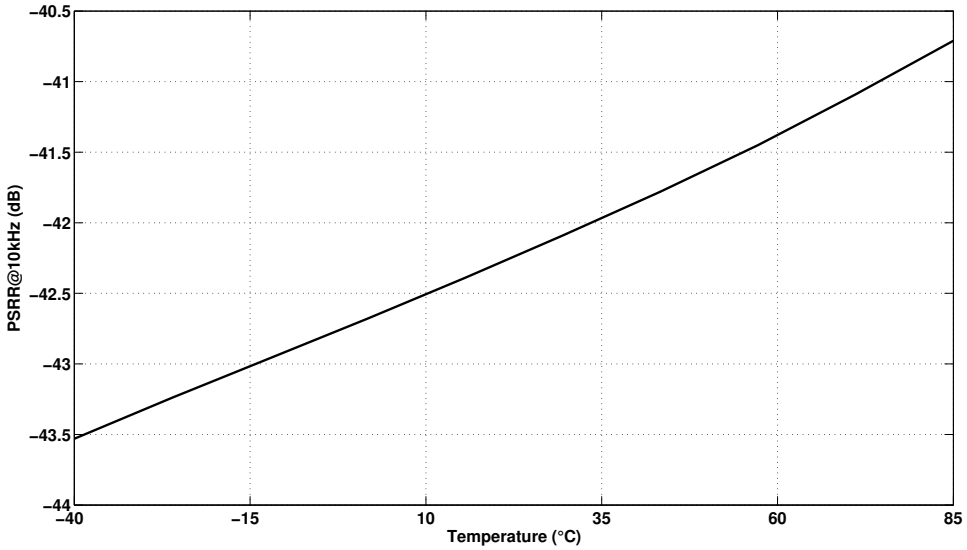


Figure 5.46: Temperature sweep of the $PSRR@10kHz$ for $I_{LOAD} = 0\ mA$.

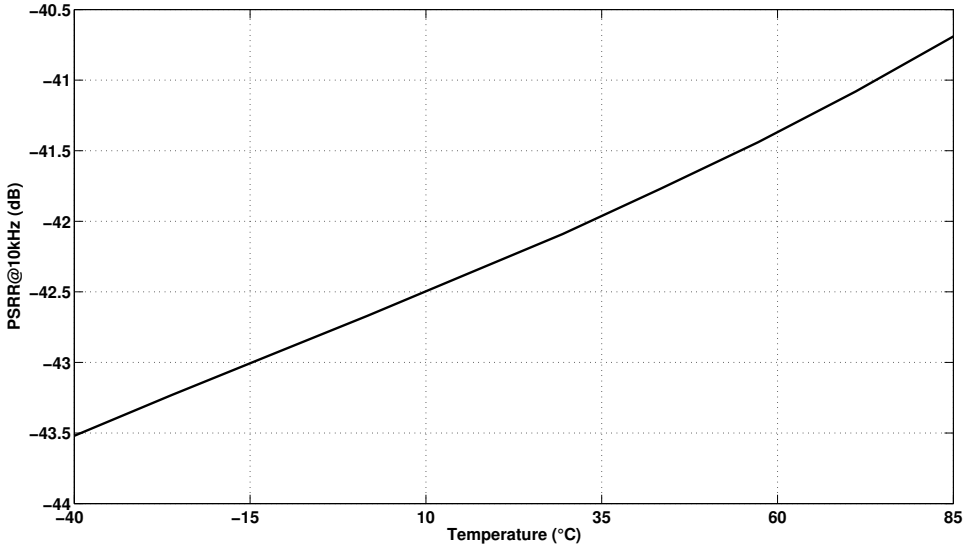


Figure 5.47: Temperature sweep of the $PSRR@10kHz$ for $I_{LOAD} = 5\ mA$.

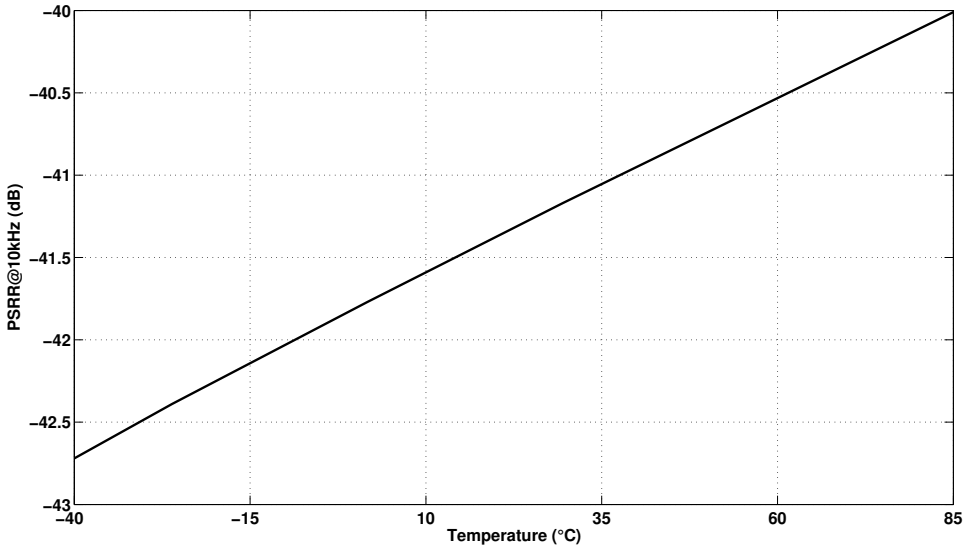


Figure 5.48: Temperature sweep of the $PSRR@10kHz$ for $I_{LOAD} = 50\ mA$.

Table 5.11: PSRR temperature sweep performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$	$\mathbf{I_{LOAD} = 5\ mA}$	$\mathbf{I_{LOAD} = 50\ mA}$
$\mathbf{TC_{PSRR@10kHz}}$ (‰/°C)	22.56	22.64	21.68

5.3.3 Monte Carlo Analysis

The monte carlo analysis of the PSRR for light-load ($I_{LOAD} = 0\ mA$), medium-load ($I_{LOAD} = 5\ mA$) and heavy-load ($I_{LOAD} = 50\ mA$) conditions is depicted in Figures

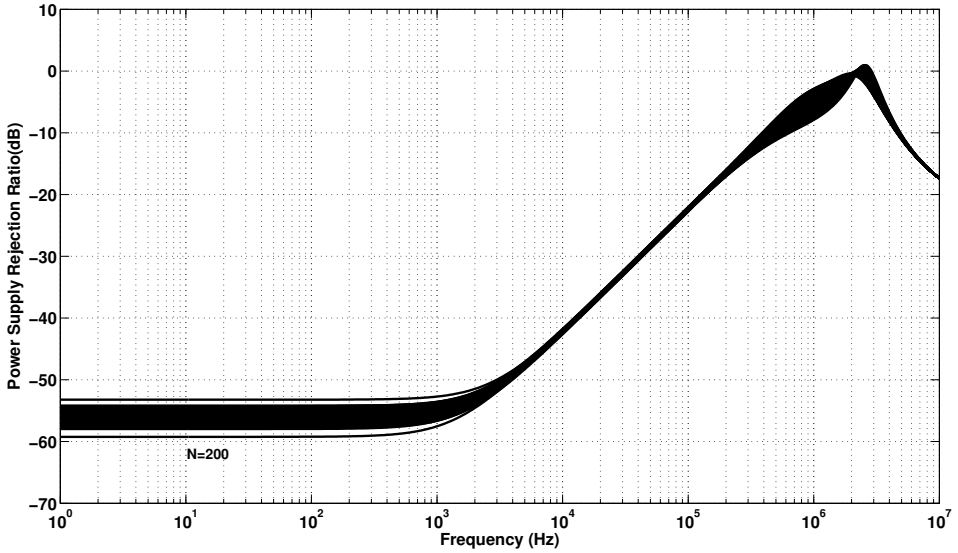


Figure 5.49: Monte carlo analysis of the PSRR for $I_{LOAD} = 0\ mA$.

5.49, 5.51 and 5.53, respectively. A zoomed-in view around around 10 kHz at each scenario is captioned in Figures 5.50, 5.52 and 5.54, respectively.

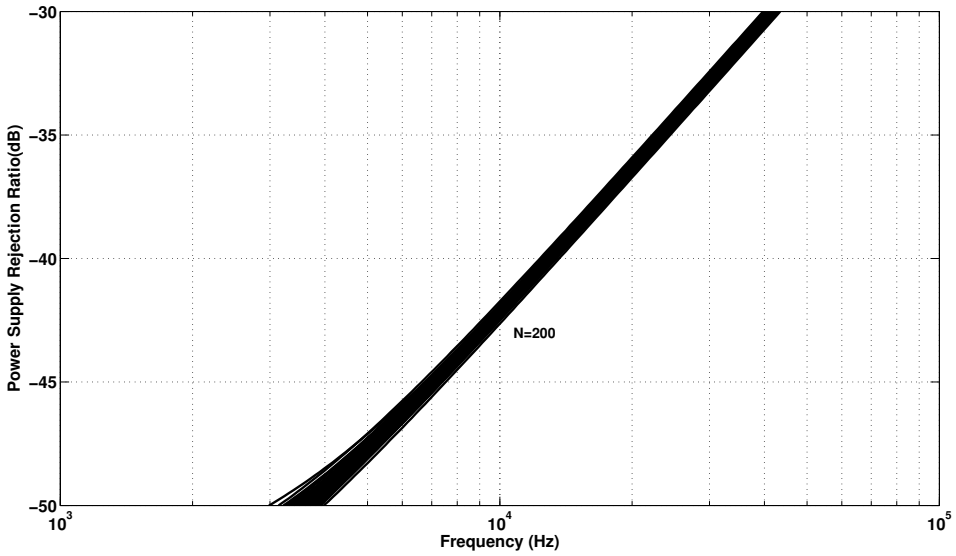


Figure 5.50: Zoomed-in view of the monte carlo analysis of the PSRR for $I_{LOAD} = 0$ mA.

At the light-load condition, the sensitivity towards fabrication process imperfections is quite low. The DC PSRR presents a variation range of about 6 dB and all samples start to pull closer to each other once the dominant pole of the system is surpassed. Hence, the specification given in Table 3.1 is met by all samples.

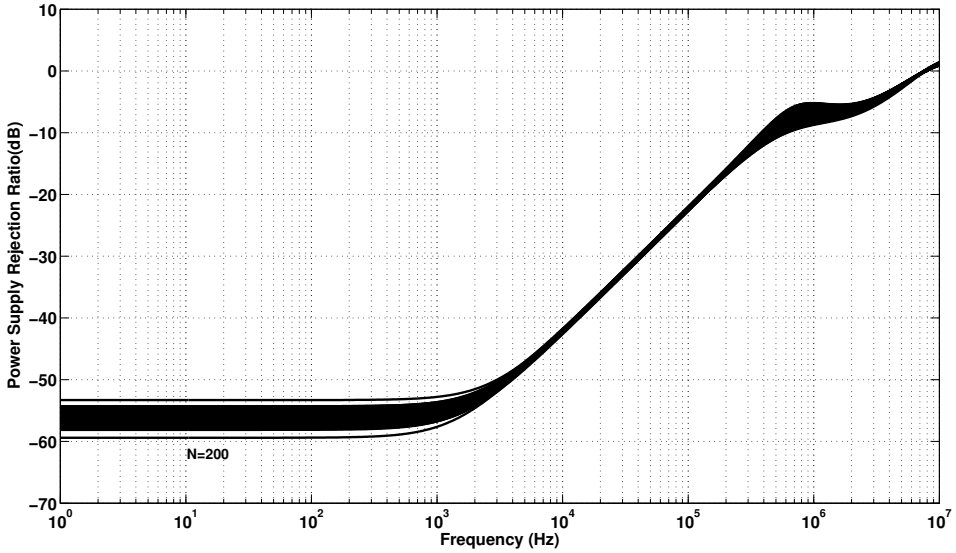


Figure 5.51: Monte carlo analysis of the PSRR for $I_{LOAD} = 5$ mA.

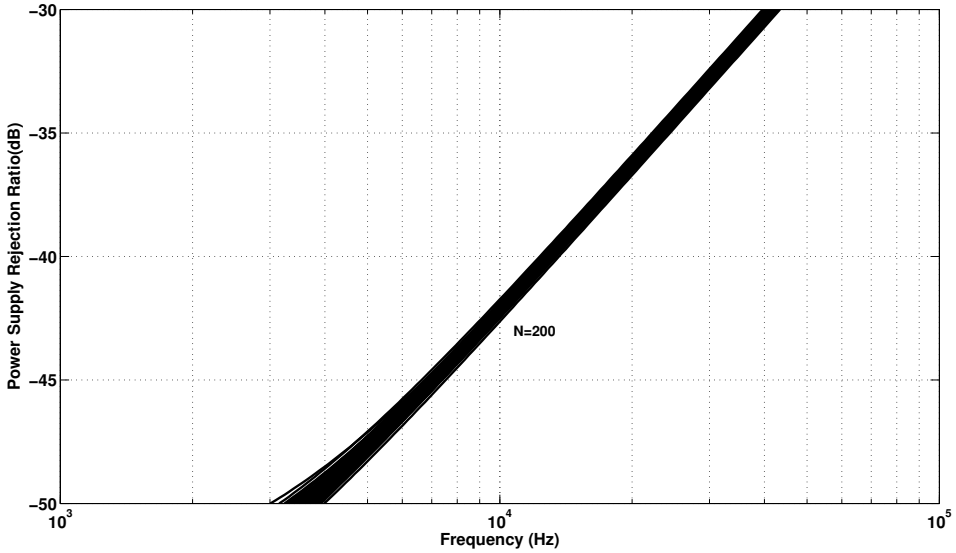


Figure 5.52: Zoomed-in view of the monte carlo analysis of the PSRR for $I_{LOAD} = 5$ mA.

At the medium-load condition, the LDO appear to be quite resilient to process parameters variations and mismatch effects as well. The behavior is very similar to the light-load condition one: the DC PSRR presents a variation range close to 6 dB and all samples start to pull closer to each other once the dominant pole of the system is surpassed. As a result, the specification given in Table 3.1 is met by all samples.

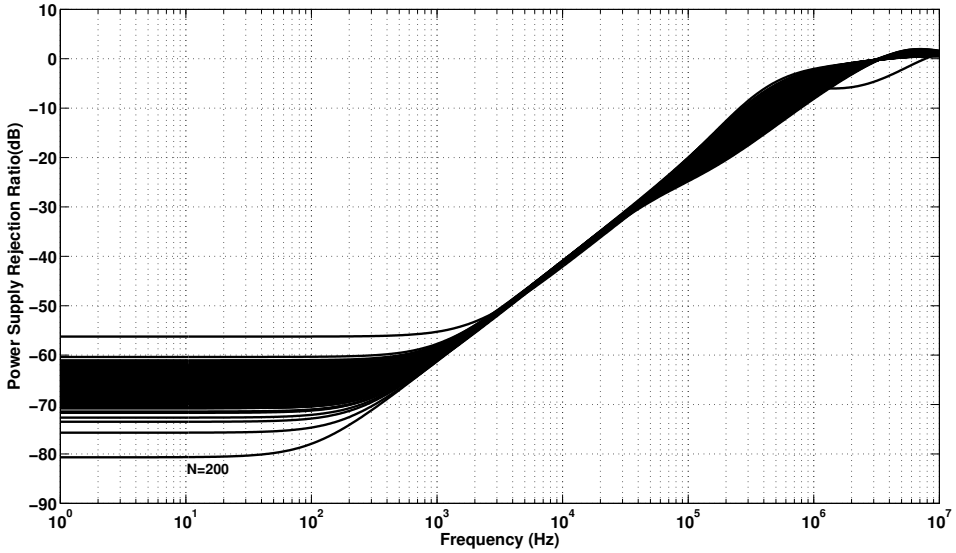


Figure 5.53: Monte carlo analysis of the PSRR for $I_{LOAD} = 50$ mA.

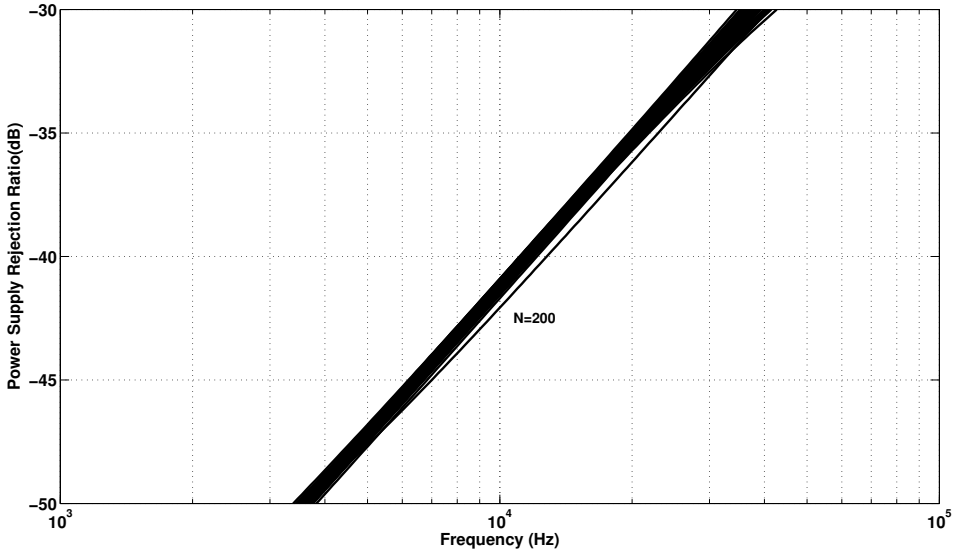


Figure 5.54: Zoomed-in view of the monte carlo analysis of the PSRR for $I_{LOAD} = 50$ mA.

At the heavy-load condition, the sensitivity towards fabrication process imperfections is quite significant. The DC PSRR presents a variation range of approximately 23 dB. However, all samples start to come together once the dominant pole of the system is surpassed. Consequently, the specification given in Table 3.1 is met by all samples.

The monte carlo analysis of the PSRR at the 10 kHz frequency for light-load, medium-load, and heavy-load conditions is illustrated in Figure 5.55, 5.56 and 5.57.

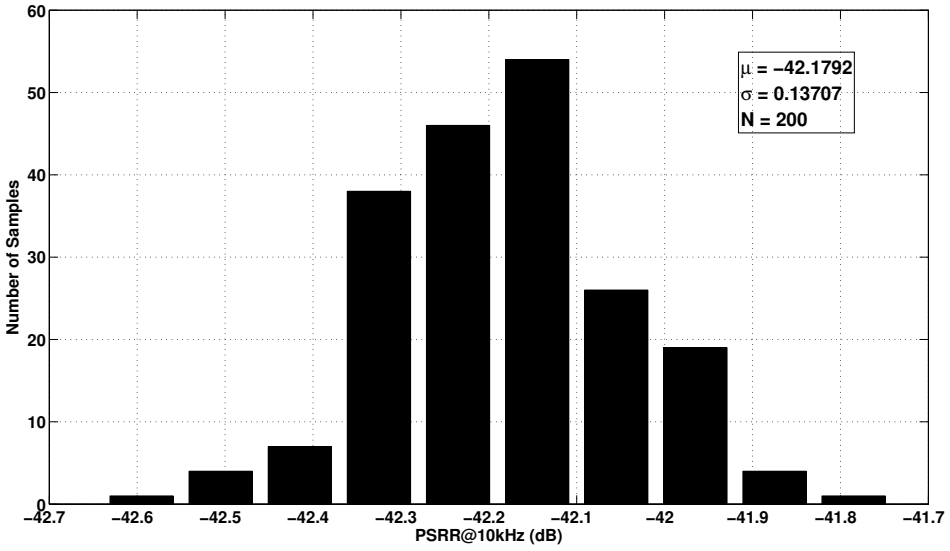


Figure 5.55: Monte carlo analysis of the $PSRR@10kHz$ for $I_{LOAD} = 0$ mA.

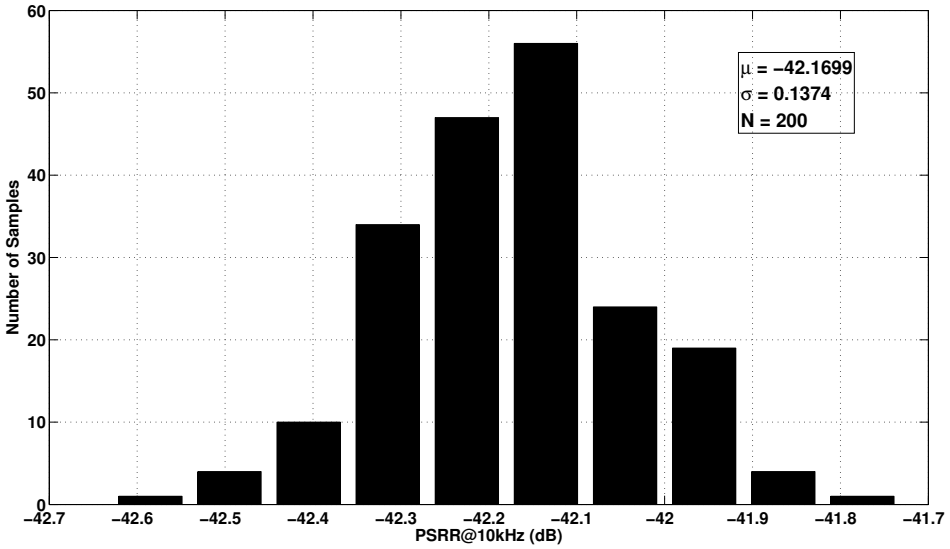


Figure 5.56: Monte carlo analysis of the $PSRR@10kHz$ for $I_{LOAD} = 5\ mA$.

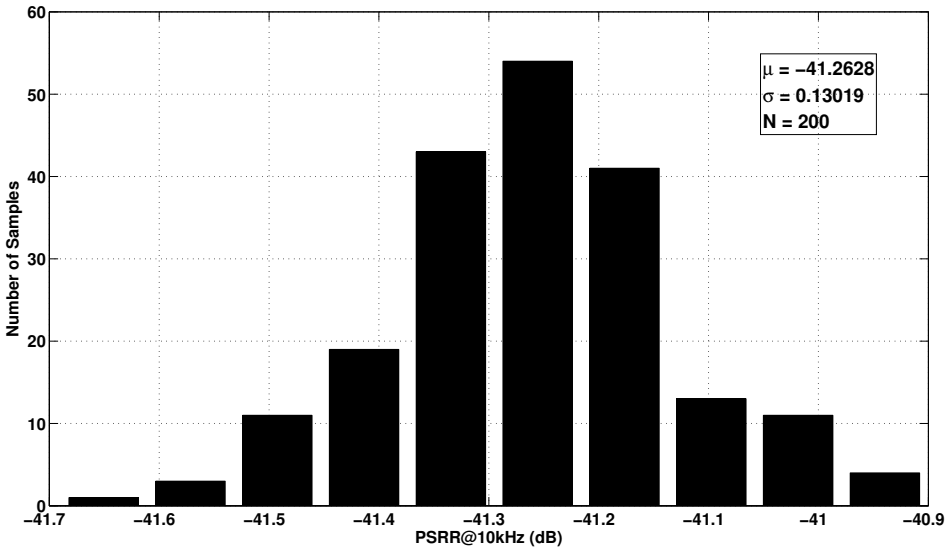


Figure 5.57: Monte carlo analysis of the $PSRR@10kHz$ for $I_{LOAD} = 50\ mA$.

The lowest value is attained at the full-load condition, but it still remains far from the -40 dB constraint. The performance summary is displayed in Table 5.12.

Table 5.12: PSRR monte carlo analysis performance summary.

	$\mathbf{I_{LOAD} = 0\ mA}$		$\mathbf{I_{LOAD} = 5\ mA}$		$\mathbf{I_{LOAD} = 50\ mA}$	
	μ	σ	μ	σ	μ	σ
PSRR@10kHz (dB)	-42.1792	0.1370	-42.1699	0.1374	-41.2628	0.1302

5.4 Load Transient Response

5.4.1 Nominal Performance

The LDO has to be able to respond to sudden full range load current changes (0 to 50 mA), such as the one depicted in Figure 5.58. For this design, the duration of both rising and falling load current shifts is of 1 μs, as it is shown in Figure 5.59.

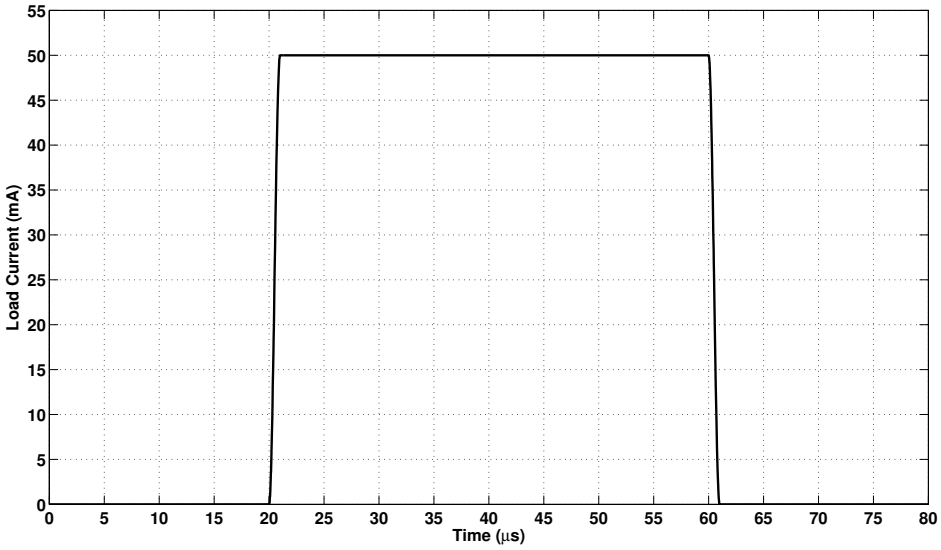


Figure 5.58: Transient load current (I_{LOAD}).

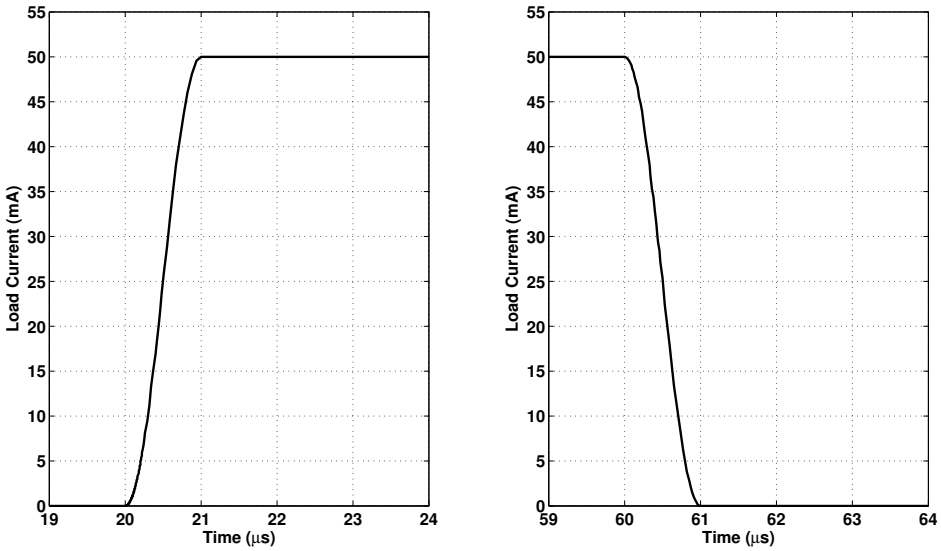


Figure 5.59: Zoomed-in view of the transient load current (I_{LOAD}).

Figure 5.60 shows how the output voltage is affected by these sudden load current

changes. It can be noticed that the overshoot presents an undershoot quality as well caused by the non-linearities of the circuit. Nevertheless, it is considered an overshoot due to the fact that the rising voltage peak is higher than the falling one. These characteristics can be easily visualized in Figure 5.61, where a zoomed-in view of the voltage peaks is captioned.

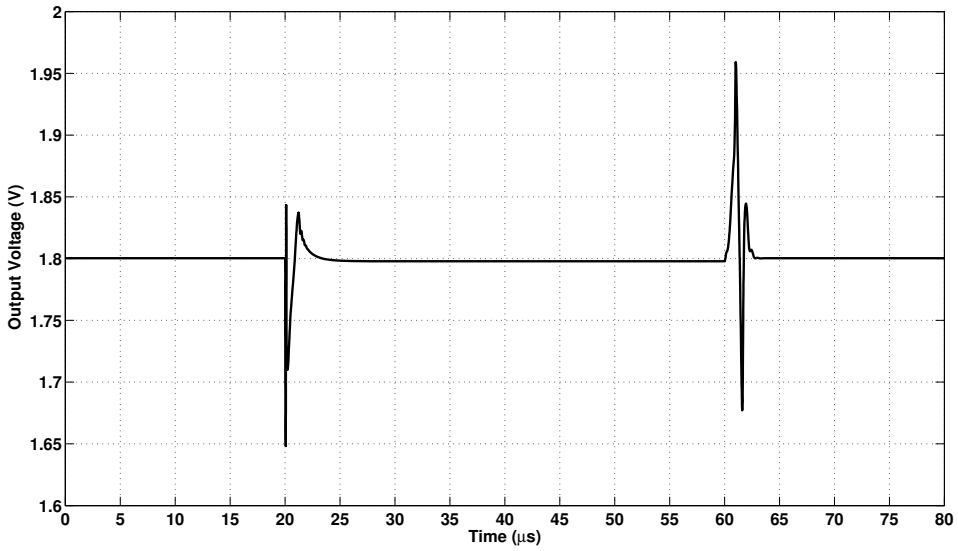


Figure 5.60: Load transient response.

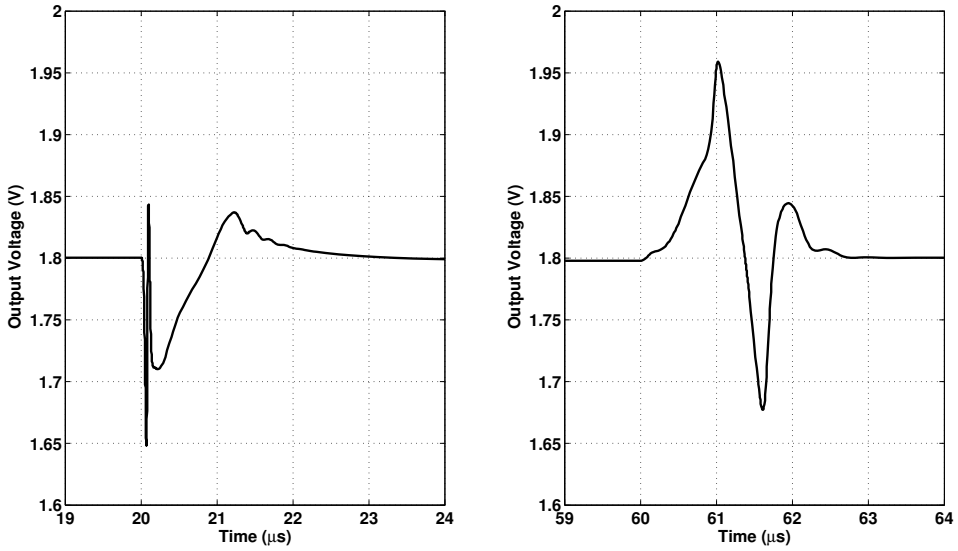


Figure 5.61: Zoomed-in view of the load transient response.

As it can be observed, the overshoot reaches its steady state a little bit faster than the undershoot. However, the undershoot magnitude is lower than the overshoot

one; though both meet the spec given in Table 3.1. The actual values are listed in Table 5.13. It is worth mentioning that the settling time was calculated considering an error of less than 0.1%.

Table 5.13: Load transient response nominal performance summary.

Undershoot ($\mathbf{\Delta V_{out_N}}$)	152.0 mV
Overshoot ($\mathbf{\Delta V_{out_P}}$)	161.3 mV
Undershoot Settling Time ($\mathbf{T_{s_N}}$)	2.737 μs
Overshoot Settling Time ($\mathbf{T_{s_P}}$)	2.641 μs

5.4.2 Temperature Sweep

Figure 5.62 shows how the load transient response varies with the temperature. A zoomed-in view around the voltage peaks is captioned in Figure 5.63.

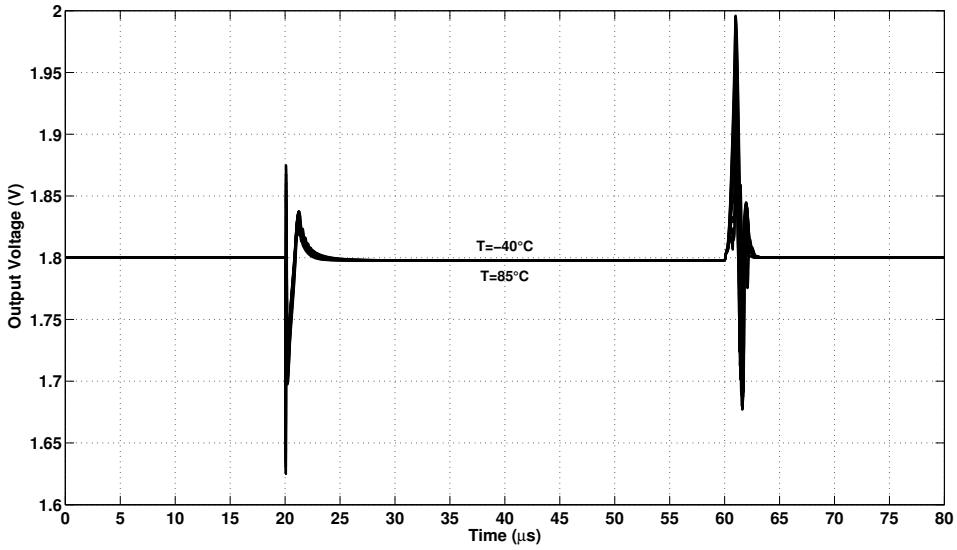


Figure 5.62: Temperature sweep of the load transient response.

As it can be visualized, the higher the temperature, the higher the voltage peaks. Furthermore, as the temperature increases, the LDO becomes slower. The temperature sweep of the load transient response performance indicators is depicted in Figure 5.64.

Most of them do not present a linear behavior. That been said, both undershoot and overshoot remain below 200 mV (spec given in Table 3.1), though the overshoot gets pretty close at the maximum temperature. The temperature coefficients of these indicators are detailed in Table 5.14.

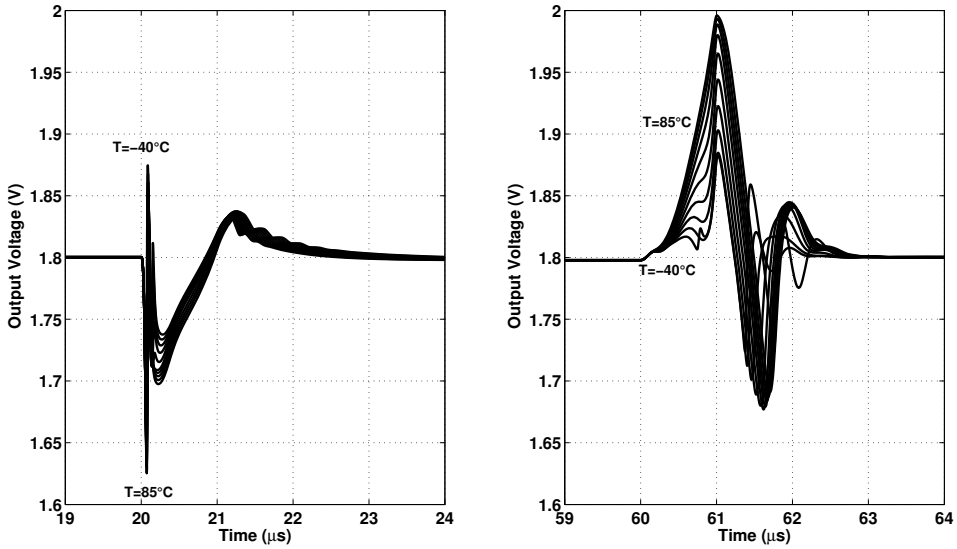


Figure 5.63: Zoomed-in view of the temperature sweep of the load transient response.

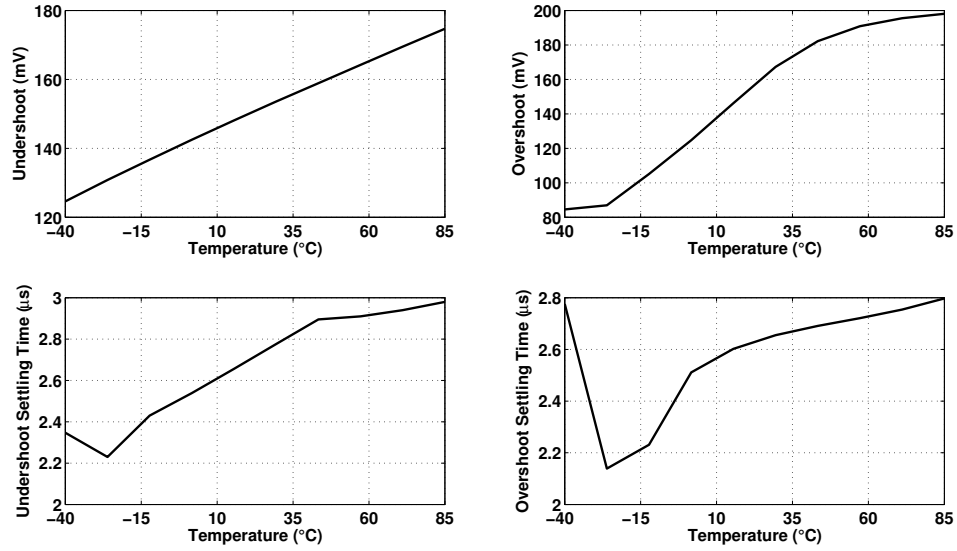


Figure 5.64: Temperature sweep of the undershoot (top left corner), overshoot (top right corner), undershoot settling time (bottom left corner), and overshoot settling time (bottom right corner).

Table 5.14: Load transient response temperature sweep performance summary.

$\mathbf{TC_{\Delta V_{out_N}}}$	0.400 ‰/°C
$\mathbf{TC_{\Delta V_{out_P}}}$	0.908 ‰/°C
$\mathbf{TC_{T_{s_N}}}$	0.0051 $ppm/°C$
$\mathbf{TC_{T_{s_P}}}$	0.0053 $ppm/°C$

5.4.3 Monte Carlo Analysis

Figure 5.65 shows the monte carlo analysis of the load transient response. A zoomed-in view around the voltage peaks is shown in Figure 5.66.

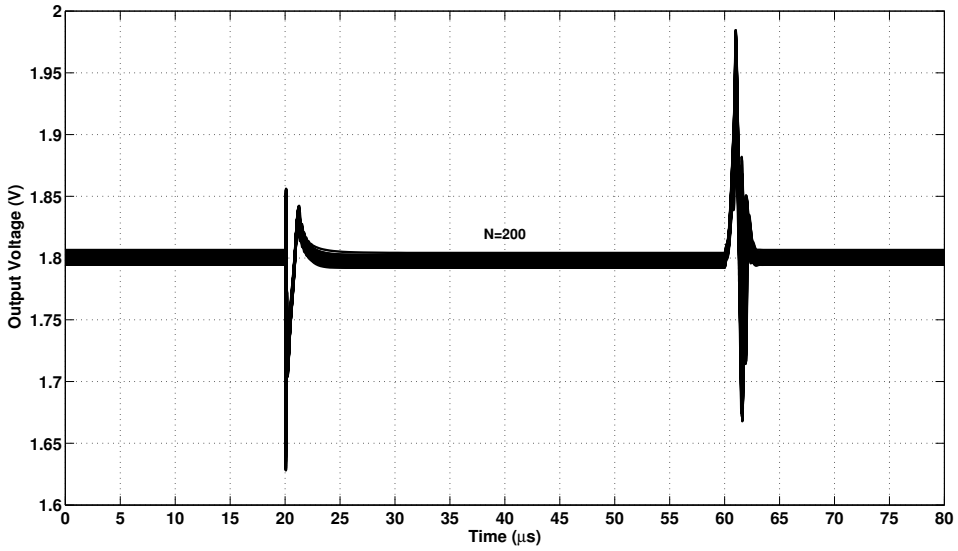


Figure 5.65: Monte carlo analysis of the load transient response.

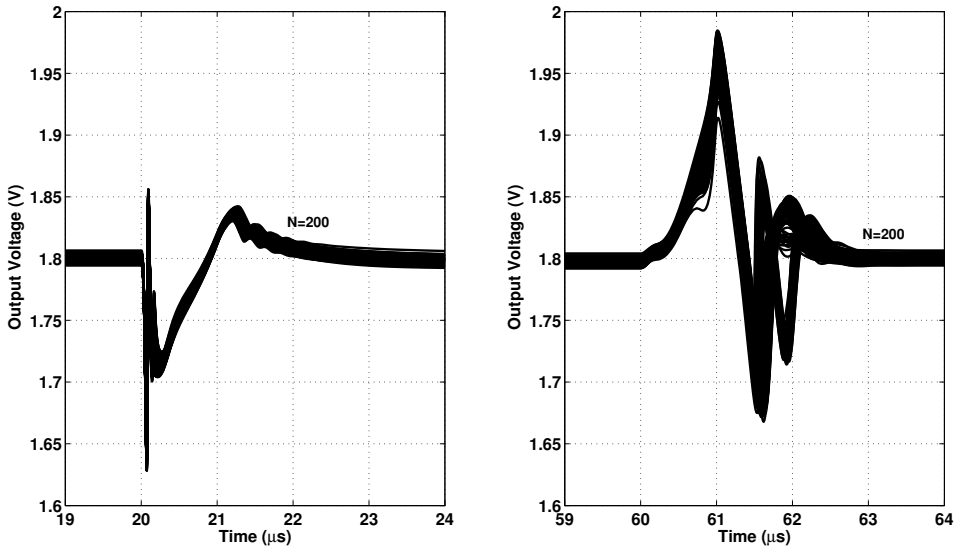


Figure 5.66: Zoomed-in view of the monte carlo analysis of the load transient response.

The undershoot and overshoot magnitudes experience minor variations. Thus, both of them remain below the 200 mV constraint given in Table 3.1. The latter, however, seems to present some tendency to an oscillatory nature. That been said,

all samples stabilize at a rather fast pace. The monte carlo analysis of the transient performance indicators is displayed in Figure 5.67. As it can be observed, both magnitude and settling time of the overshoot present a higher variation range than its respective counterparts. The performance summary is detailed in Table 5.15.

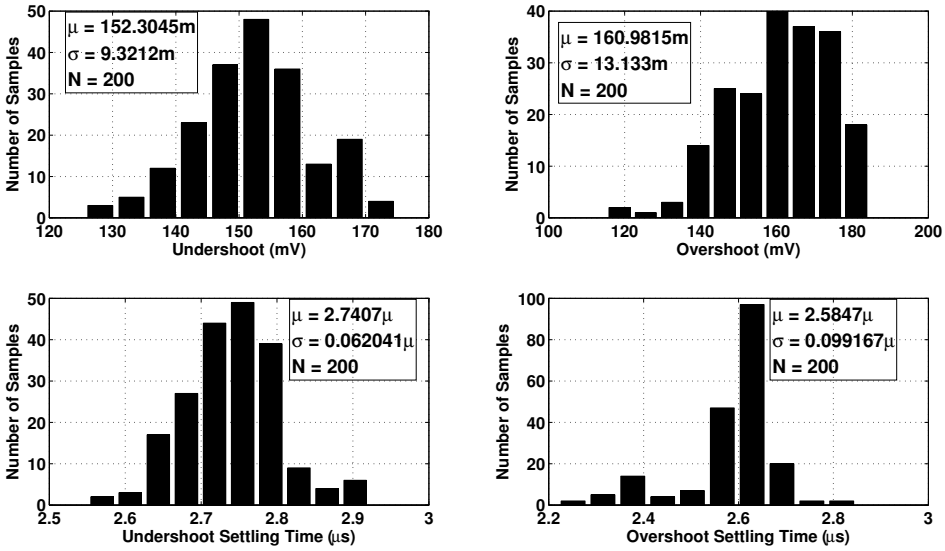


Figure 5.67: Monte carlo analysis of the undershoot (top left corner), overshoot (top right corner), undershoot settling time (bottom left corner), and overshoot settling time (bottom right corner).

Table 5.15: Load transient response monte carlo analysis performance summary.

$\mathbf{\Delta V_{out_N}}$	$\mu = 152.30\ mV$	$\sigma = 9.32\ mV$
$\mathbf{\Delta V_{out_P}}$	$\mu = 160.98\ mV$	$\sigma = 13.13\ mV$
$\mathbf{T_{s_N}}$	$\mu = 2.741\ \mu s$	$\sigma = 0.062\ \mu s$
$\mathbf{T_{s_P}}$	$\mu = 2.585\ \mu s$	$\sigma = 0.099\ \mu s$

5.5 Load Regulation

5.5.1 Nominal Performance

Figure 5.68 shows how the output voltage varies according to the load current. As it can be observed, the behavior is pretty linear and the variation range is around 2.5 mV. This is mainly caused by the parasitic resistances associated with the metal paths and vias employed in the layout design of the power transistor. The actual load regulation coefficient (LoR) is displayed in Table 5.16 and expressed as

$$LoR = \frac{\Delta V_{out}}{\Delta I_{LOAD}} = \frac{V_{out_{max}} - V_{out_{min}}}{I_{LOAD_{max}} - I_{LOAD_{min}}}. \tag{5.2}$$

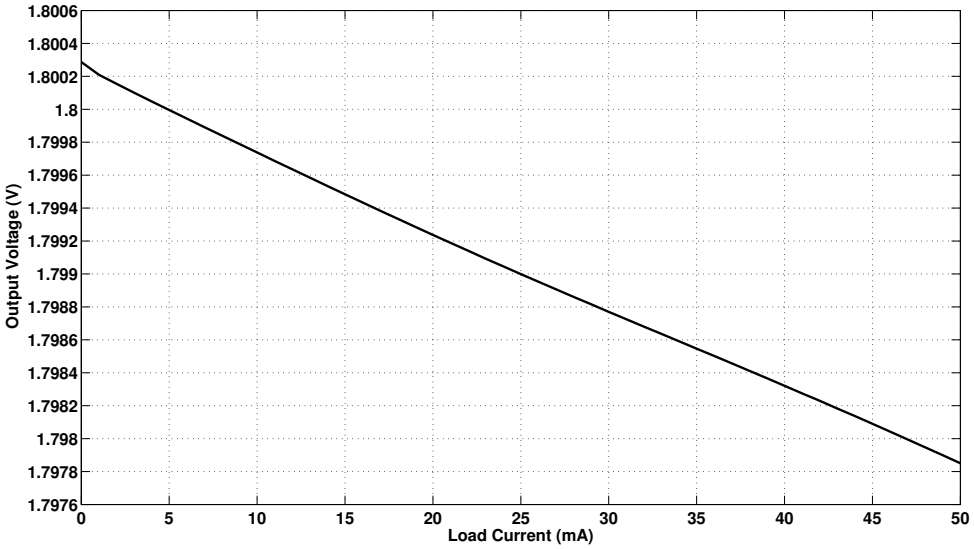


Figure 5.68: Load regulation.

Table 5.16: Load regulation nominal performance summary.

Load Regulation (LoR)	$0.0487\ mV/mA$

5.5.2 Temperature Sweep

Figure 5.69 shows how the load regulation varies according to the temperature.

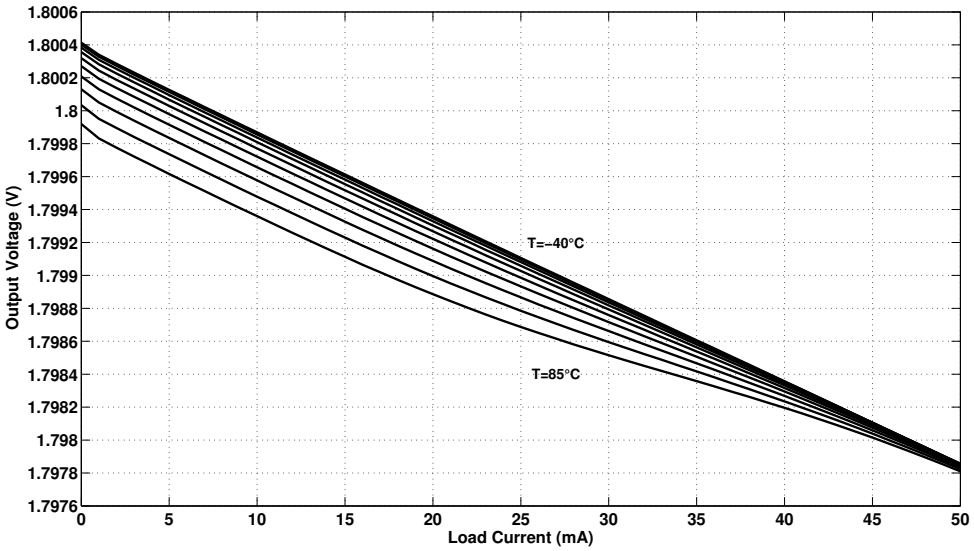


Figure 5.69: Temperature sweep of the load regulation.

As it can be observed, the variation range of the output voltage diminishes as the temperature enlarges. Consequently, the load regulation becomes more accurate with higher temperatures. Nevertheless, the actual slope difference between all the load regulation curves is relatively small.

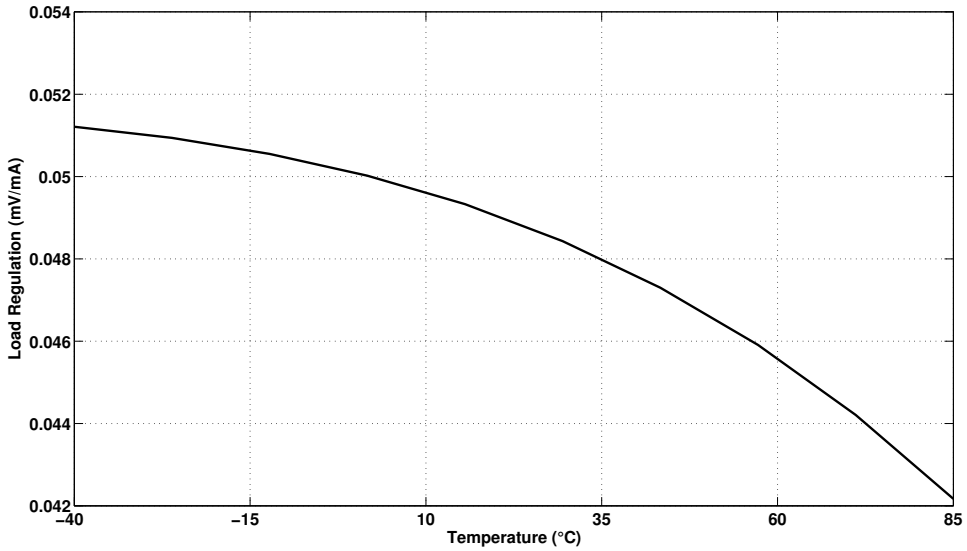


Figure 5.70: Temperature sweep of the load regulation coefficient (LoR).

The LoR temperature dependent variation can be better appreciated in Figure 5.70. As it can be visualized, the worst case scenario (highest value) takes place at the lowest temperature, as it was expected. The LoR temperature coefficient is listed in Table 5.17.

Table 5.17: Load regulation temperature sweep performance summary.

$\mathbf{TC_{LoR}}$	$72.32\ ppm/°C$

5.5.3 Monte Carlo Analysis

Figure 5.71 shows the monte carlo analysis of the load regulation. As it can be visualized, the fabrication process imperfections have a deep impact on the DC level of the preset output voltage. However, its load regulation remains highly resilient to the aforementioned phenomenon, as it can be verified in Figure 5.72. The performance summary is detailed in Table 5.17.

Table 5.18: Load regulation monte carlo analysis performance summary.

LoR	$\mu = 0.0487\ mV/mA$	$\sigma = 0.0004\ mV/mA$

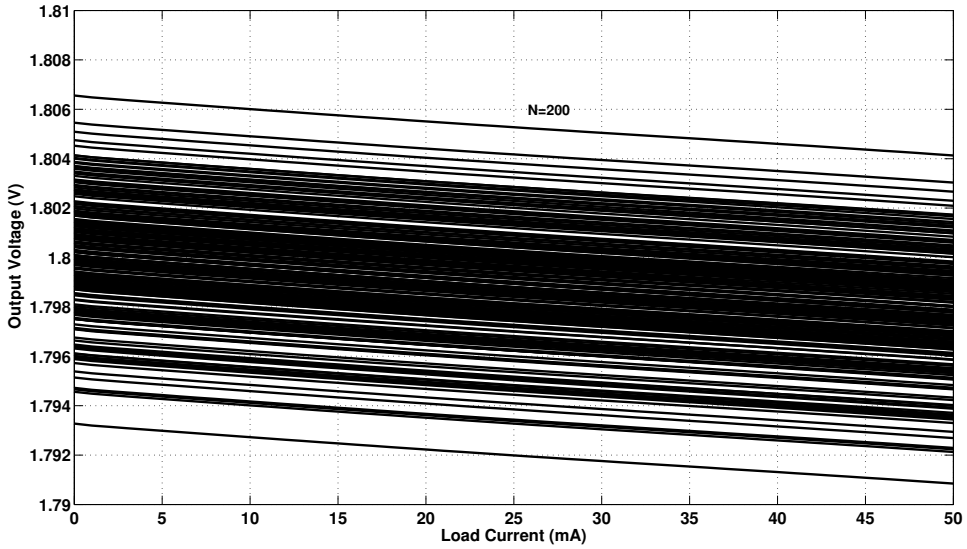


Figure 5.71: Monte carlo analysis of the load regulation.

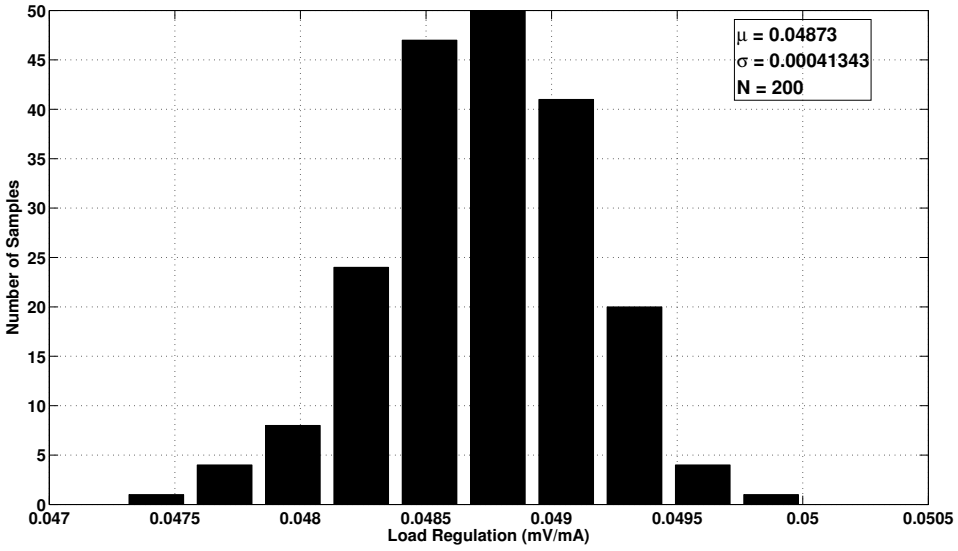


Figure 5.72: Monte carlo analysis of the load regulation coefficient (LoR).

5.6 Line Transient Response

5.6.1 Nominal Performance

The LDO has to be able to withstand sudden full range input supply voltage changes (2 to 2.5 V), such as the one depicted in Figure 5.73. For this specific design, the duration of both rising and falling input supply voltage shifts is of 5 μs, as it is shown in Figure 5.74. Moreover, the scenario to be analyzed is the full-load condition

($I_{LOAD} = 50\ mA$) since is the most critical one.

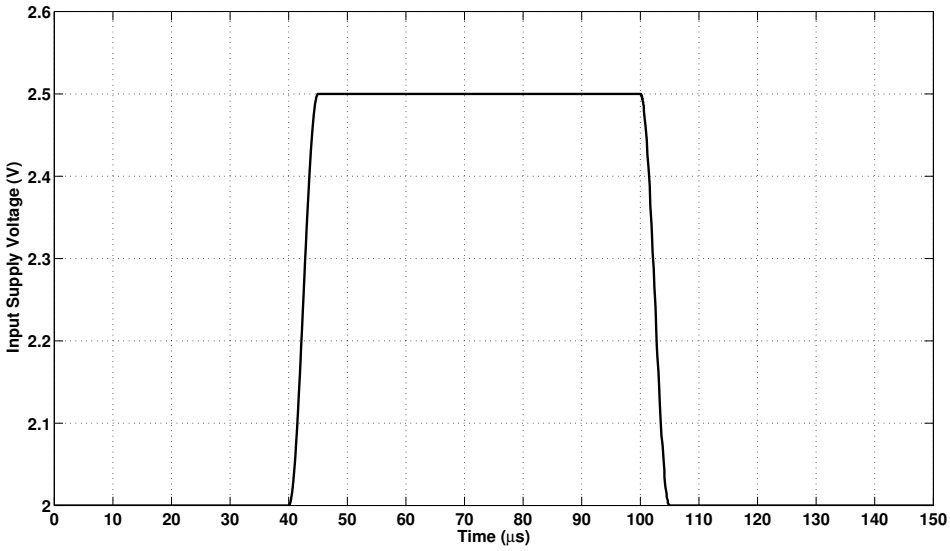


Figure 5.73: Transient input supply voltage (V_{supp}).

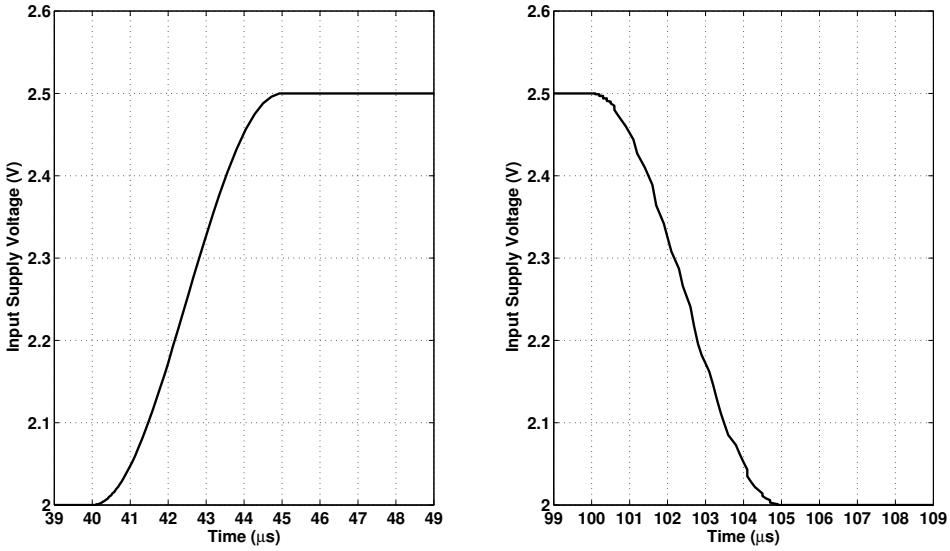


Figure 5.74: Zoomed-in view of the transient input supply voltage (V_{supp}).

Figure 5.75 shows how the output voltage is affected by these sudden input supply voltage changes. A zoomed-in view of the voltage peaks is captioned Figure 5.76. As it can be observed, the undershoot reaches its steady state a little bit faster than the overshoot. Nevertheless, the overshoot magnitude is lower than the undershoot one; though both meet the spec given in Table 3.1. The actual values are

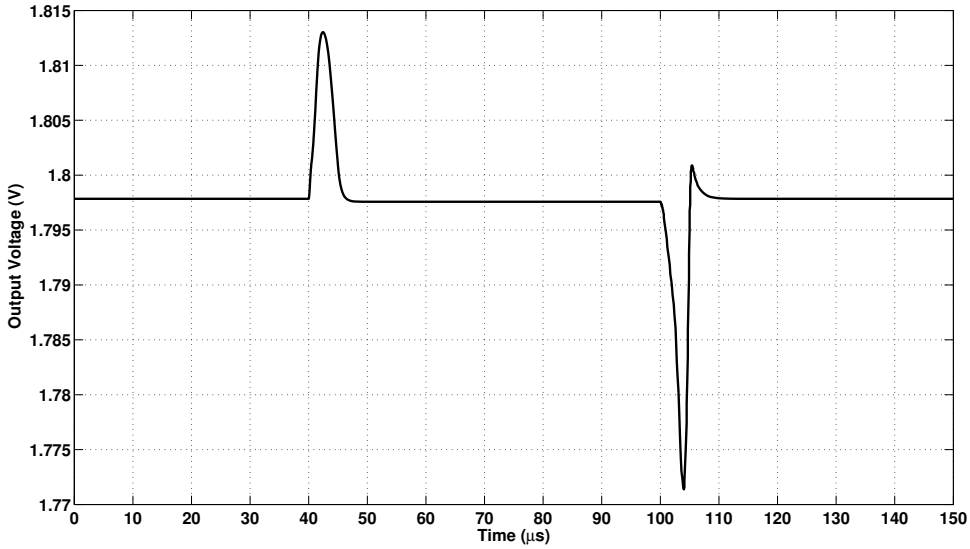


Figure 5.75: Line transient response.

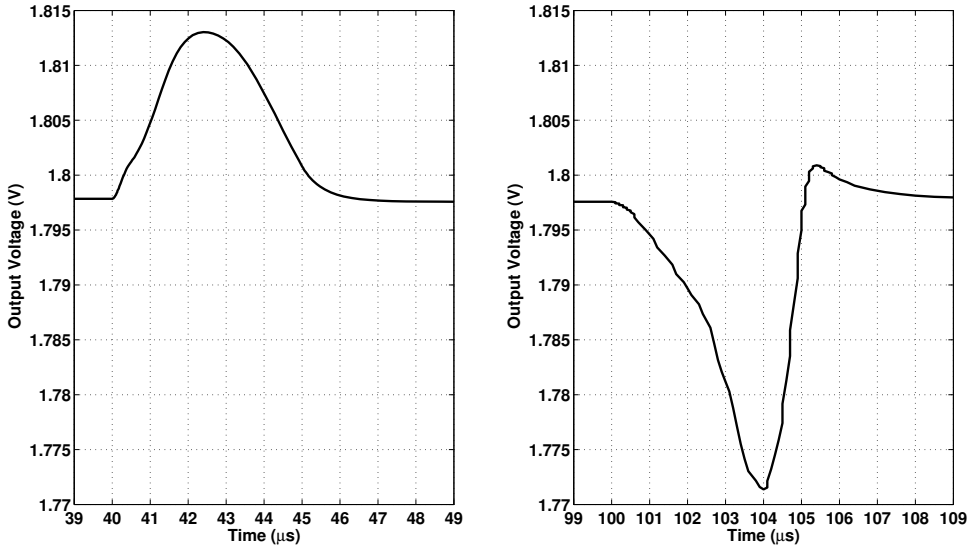


Figure 5.76: Zoomed-in view of the line transient response.

displayed in Table 5.19. In this scenario, an error of less than 0.1% was considered for the settling time calculation.

Table 5.19: Line transient response nominal performance summary.

Overshoot ($\mathbf{\Delta V_{out_P}}$)	15.18 mV
Undershoot ($\mathbf{\Delta V_{out_N}}$)	26.20 mV
Overshoot Settling Time ($\mathbf{T_{s_P}}$)	5.322 μs
Undershoot Settling Time ($\mathbf{T_{s_N}}$)	5.126 μs

5.6.2 Temperature Sweep

Figure 5.77 shows how the line transient response varies with the temperature. A zoomed-in view around the voltage peaks is captioned in Figure 5.78.

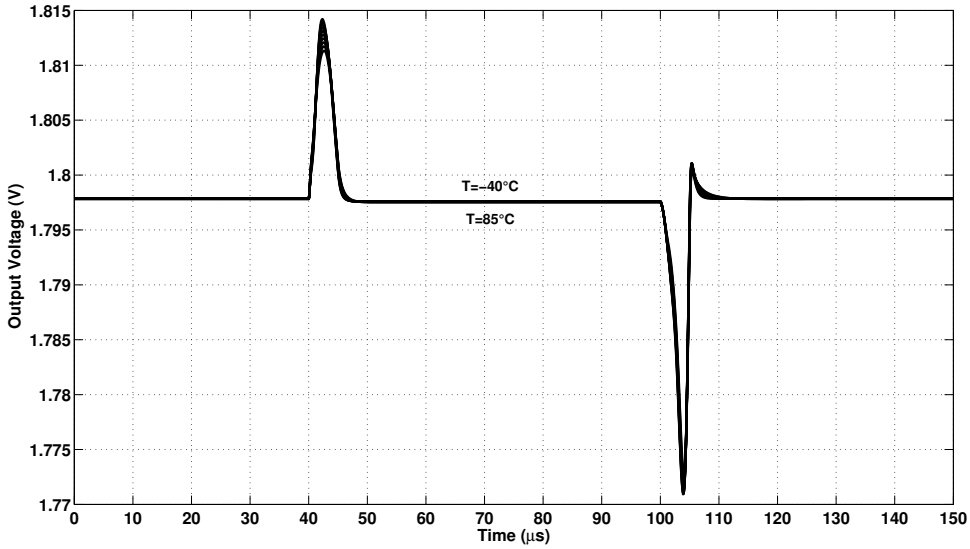


Figure 5.77: Temperature sweep of the line transient response.

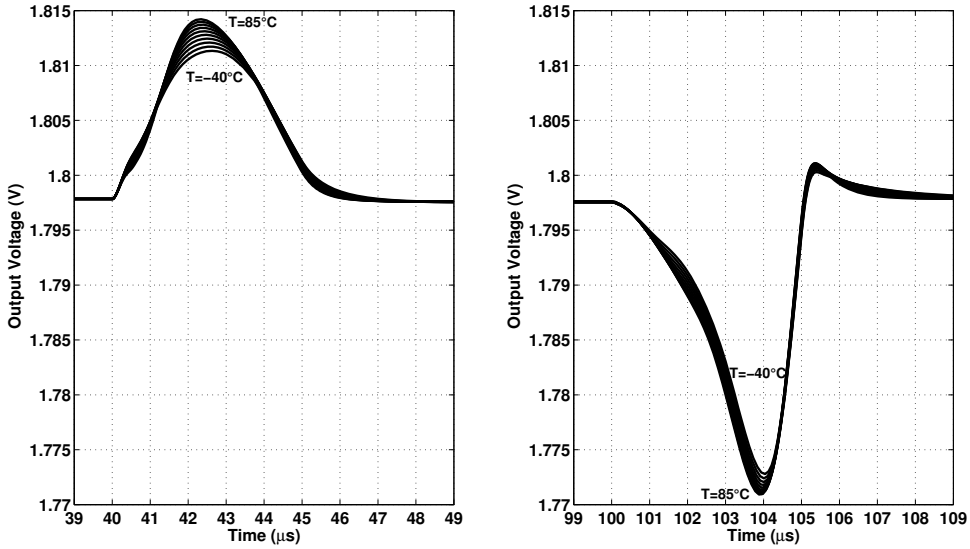


Figure 5.78: Zoomed-in view of the temperature sweep of the line transient response.

As it can be noticed, the line transient response experience the same effect as the load one: the higher the temperature, the higher the voltage peaks. The temperature sweep of the line transient response performance indicators is depicted in Figure 5.79. The temperature coefficients of these indicators are detailed in Table 5.20.

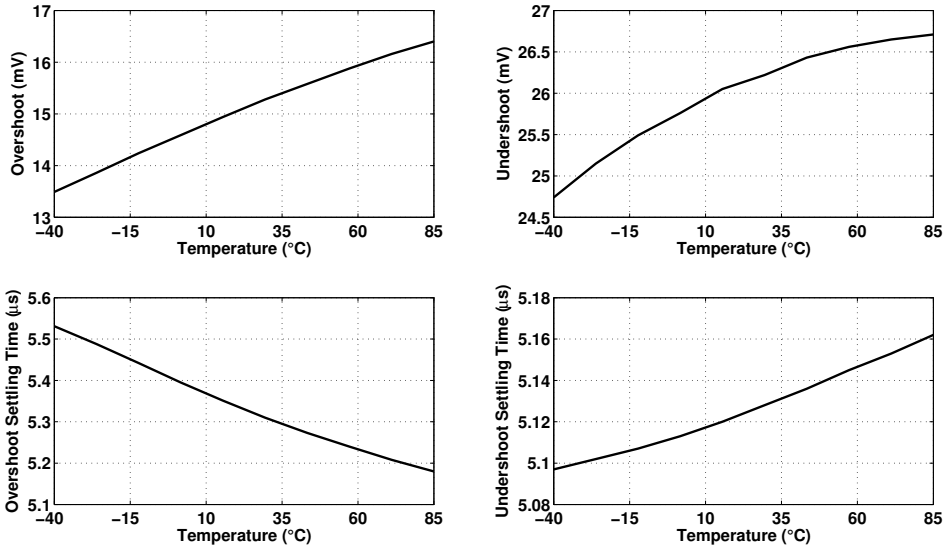


Figure 5.79: Temperature sweep of the overshoot (top left corner), undershoot (top right corner), overshoot settling time (bottom left corner), and undershoot settling time (bottom right corner).

Table 5.20: Line transient response temperature sweep performance summary.

$\mathbf{TC_{\Delta V_{out_P}}}$	23.28 $ppm/°C$
$\mathbf{TC_{\Delta V_{out_N}}}$	15.76 $ppm/°C$
$\mathbf{TC_{T_{s_P}}}$	0.0028 $ppm/°C$
$\mathbf{TC_{T_{s_N}}}$	0.0005 $ppm/°C$

5.6.3 Monte Carlo Analysis

Figure 5.80 shows the monte carlo analysis of the line transient response. A zoomed-in view around the voltage peaks is shown in Figure 5.81. As it can be noticed, the overshoot and undershoot magnitudes experience a relatively significant variation. Nevertheless, the worst case scenarios for both parameters are still non-threatening to the normal operation of the LDO. Furthermore, the speed of the LDO appears to be highly resilient to process variations and mismatch effects.

Figure 5.82 displays the monte carlo analysis of the transient response performance indicators. As it can be visualized, the variation range of the undershoot magnitude highly surpasses the one of the overshoot. However, the former presents a much more gaussian-like distribution than the latter. On the other hand, the variation range of the overshoot settling time exceeds significantly the undershoot one. Nevertheless, the former presents a less scattered performance than the latter. The performance summary is detailed in Table 5.21.

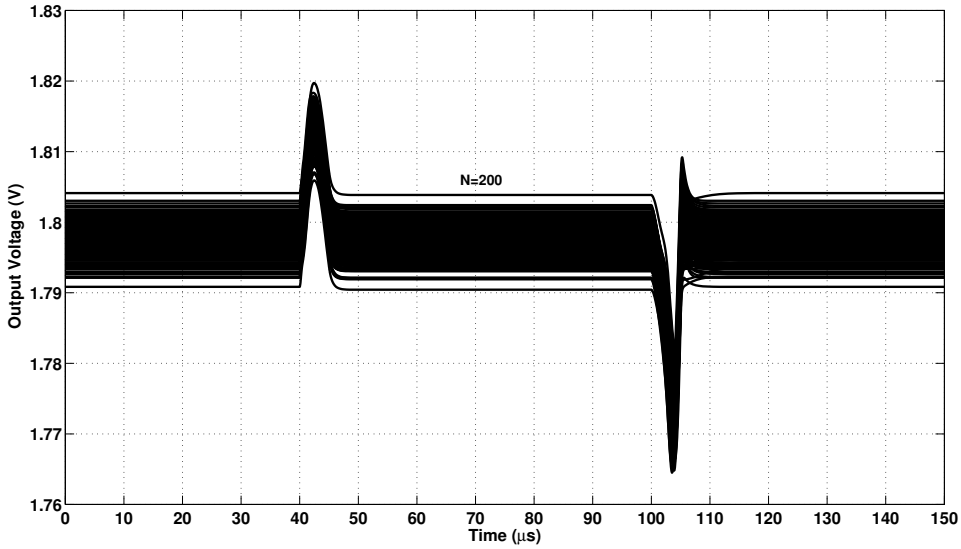


Figure 5.80: Monte carlo analysis of the line transient response.

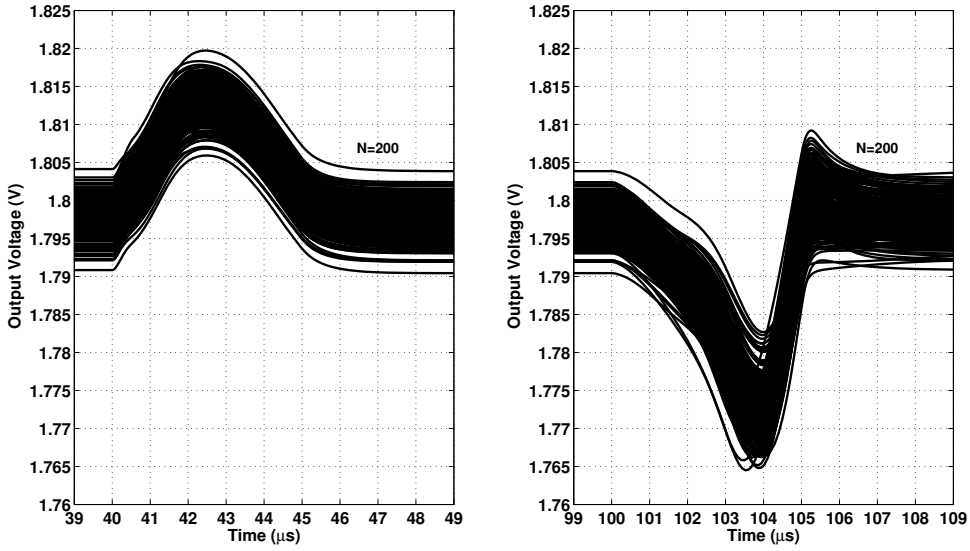


Figure 5.81: Zoomed-in view of the monte carlo analysis of the line transient response.

Table 5.21: Line transient response monte carlo analysis performance summary.

$\mathbf{\Delta V_{out_P}}$	$\mu = 15.15\ mV$	$\sigma = 0.24\ mV$
$\mathbf{\Delta V_{out_N}}$	$\mu = 25.13\ mV$	$\sigma = 3.31\ mV$
$\mathbf{T_{s_P}}$	$\mu = 5.317\ \mu s$	$\sigma = 0.129\ \mu s$
$\mathbf{T_{s_N}}$	$\mu = 5.064\ \mu s$	$\sigma = 0.116\ \mu s$

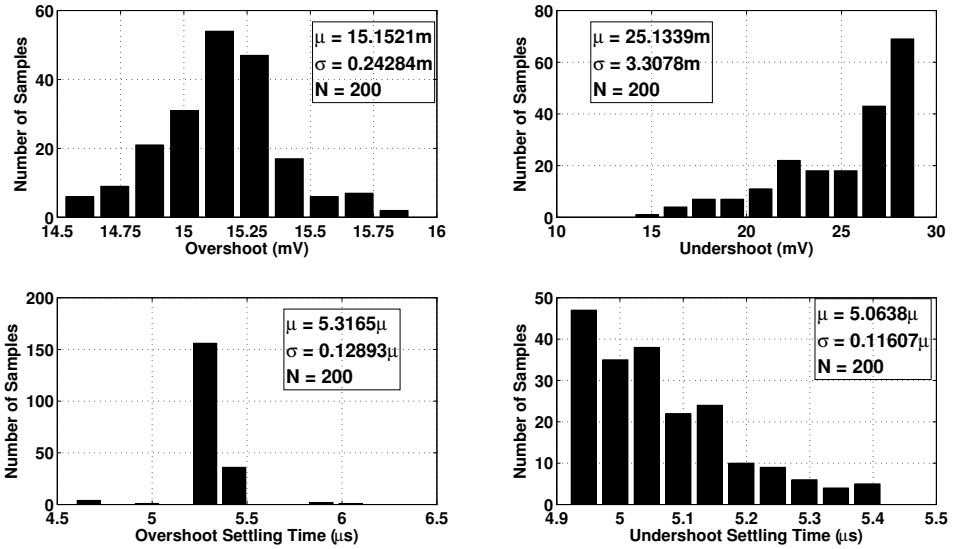


Figure 5.82: Monte carlo analysis of the overshoot (top left corner), undershoot (top right corner), overshoot settling time (bottom left corner), and undershoot settling time (bottom right corner).

5.7 Line Regulation

5.7.1 Nominal Performance

Figure 5.83 shows how the output voltage varies according to the input supply voltage (assuming $I_{LOAD} = 50\ mA$).

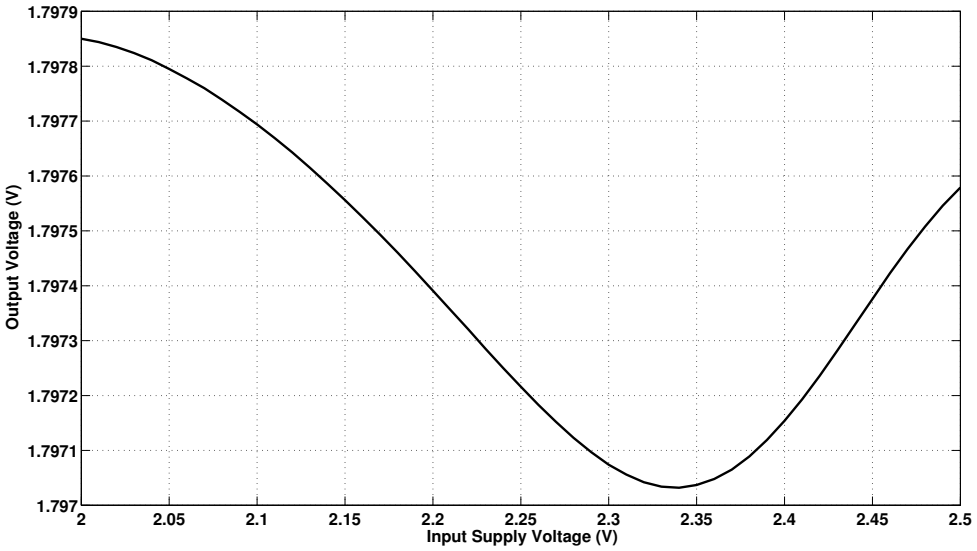


Figure 5.83: Line regulation.

As it can be noticed, the behavior is not quite linear, which is to be expected due to the non-linear adaptive nature of the circuit. The maximum variation is around 0.8 mV. The actual line regulation coefficient (LiR) is expressed in Table 5.22 and described by

$$LiR = \frac{\Delta V_{out}}{\Delta V_{supp}} = \frac{V_{out_{max}} - V_{out_{min}}}{V_{supp_{max}} - V_{supp_{min}}}. \tag{5.3}$$

Table 5.22: Line regulation nominal performance summary.

Line Regulation (LiR)	1.636 mV/V

5.7.2 Temperature Sweep

Figure 5.84 shows how the line regulation varies according to the temperature.

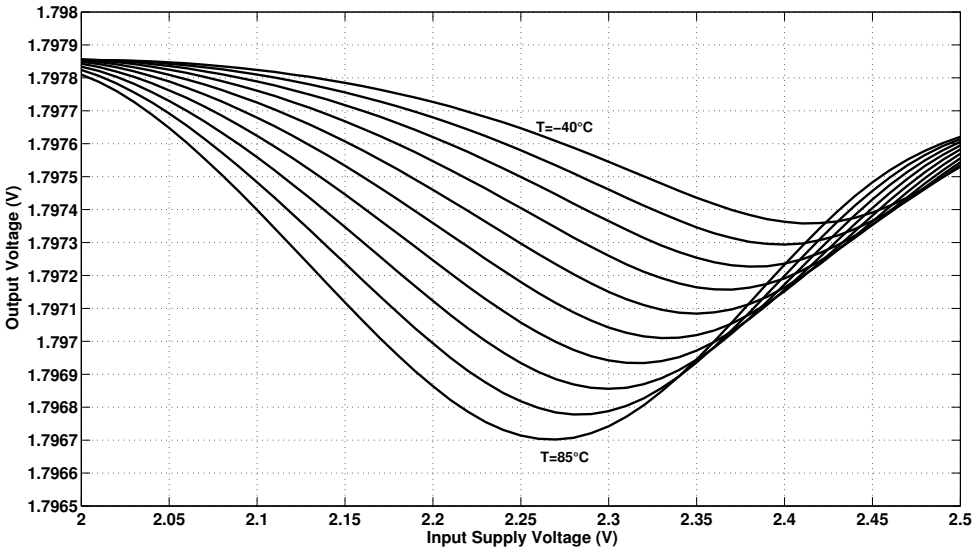


Figure 5.84: Temperature sweep of the line regulation.

The variation range of the output voltage rises as the temperature enlarges. Consequently, the line regulation becomes more accurate with lower temperatures. The LiR temperature dependent variation can be better appreciated in Figure 5.85. As it can be noticed, the worst case scenario takes place at the highest temperature. The LiR temperature coefficient is listed in Table 5.23.

Table 5.23: Line regulation temperature sweep performance summary.

$\mathbf{TC_{LiR}}$	9.808 $ppm/°C$

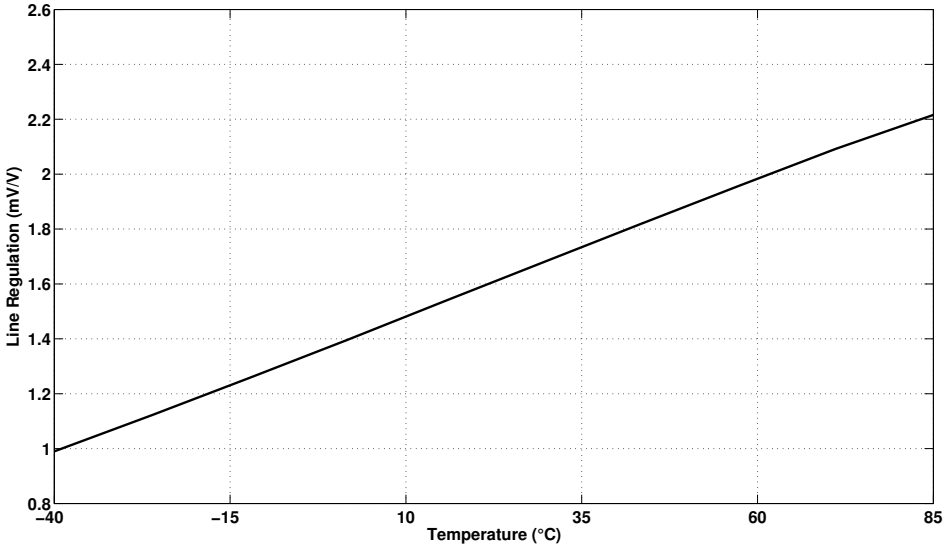


Figure 5.85: Temperature sweep of the line regulation coefficient (LiR).

5.7.3 Monte Carlo Analysis

Figure 5.86 shows the monte carlo analysis of the line regulation.

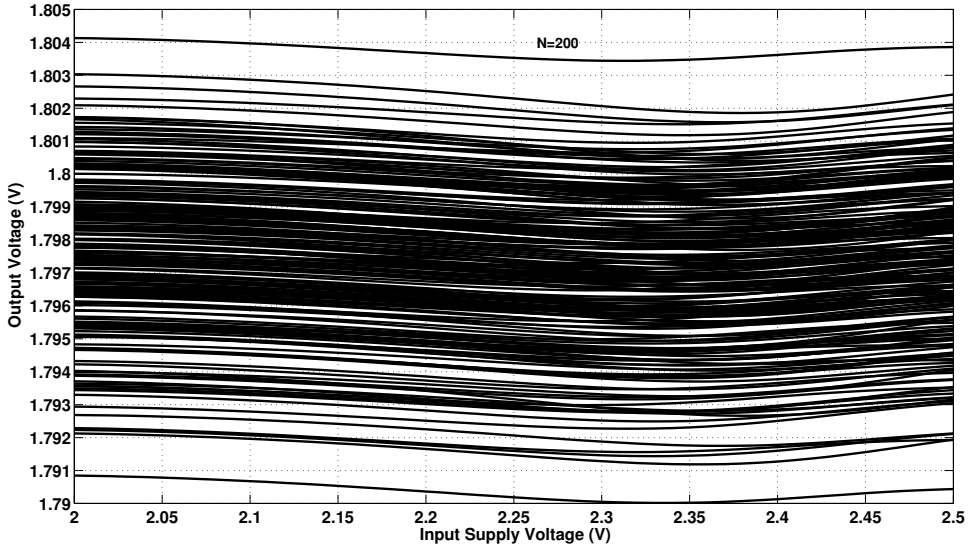


Figure 5.86: Monte carlo analysis of the line regulation.

As mentioned before, the process variations and mismatch effects have a considerable impact on the DC level of the output voltage. Nonetheless, the line regulation is not nearly as sensitive to this phenomenon, as it can be corroborated in Figure 5.87. The performance summary is displayed in Table 5.24.

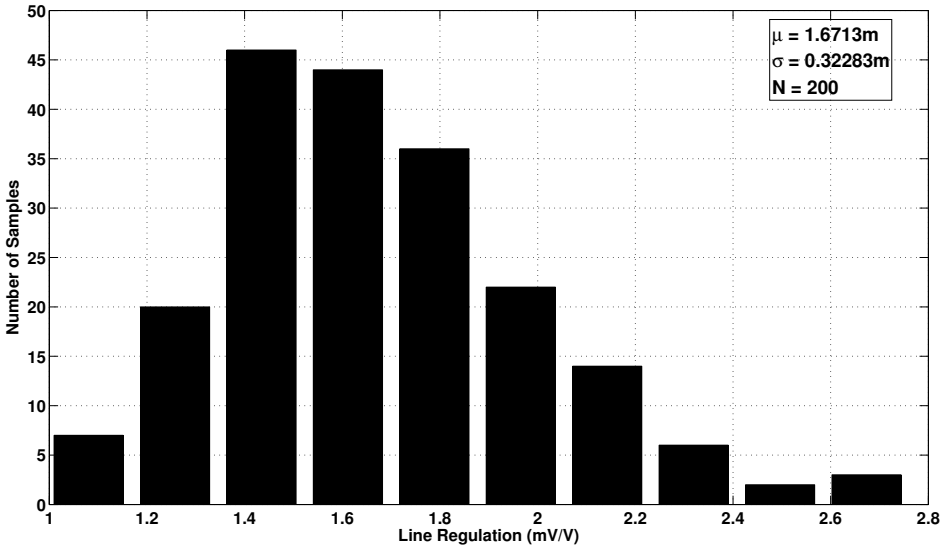


Figure 5.87: Monte carlo analysis of the line regulation coefficient (LiR).

Table 5.24: Line regulation monte carlo analysis performance summary.

LiR	$\mu = 1.671\ mV/V$	$\sigma = 0.323\ mV/V$

5.8 Performance Summary

The main features of the LDO performance have been summarized in Table 5.25. The transient indicators refer to the load analysis and represent the highest occurrence. The temperature coefficient refers to the output voltage.

Table 5.25: LDO performance summary.

Technology	IBM 0.18μm
Active Chip Area	295.25 μm × 209.57 μm
On-chip Capacitance	6.3 pF
Output Capacitance (C_{out})	50 pF
Input Supply Voltage (V_{supp})	2.0-2.5 V
Preset Output Voltage (V_{out})	1.8 V
Output Load Current (I_{LOAD})	0-50 mA
Dropout Voltage (V_{DO})	200 mV @ $I_{LOAD} = 50\ mA$
Quiescent Current (I_Q)	58 μA
PSRR	-41.21 dB @ 10 kHz, $I_{LOAD} = 50\ mA$
Load Regulation (LoR)	0.0487 mV/mA @ $V_{supp} = 2\ V$
Line Regulation (LiR)	1.636 mV/V @ $I_{LOAD} = 50\ mA$
Edge Time (Δt)	1 μs
Settling Time (T_s)	2.74 μs @ 0.1% error, $V_{supp} = 2\ V$
Output Voltage Peak (ΔV_{out})	161.3 mV @ $V_{supp} = 2\ V$
Temperature Coefficient	0.336 $ppm/°C$ @ $I_{LOAD} = 50\ mA$

Chapter 6

Conclusions

6.1 General Conclusions

The entire design of an output-capacitorless LDO was presented in this dissertation. The design features an innovative adaptive active feedback compensation scheme, a slew rate enhancement block and a dynamic biasing path that allow for a highly stable, accurate and fast state-of-the-art LDO.

The adaptive active feedback compensation scheme was introduced in this dissertation. The circuit prove to modify the frequency response of the LDO according to the load requirements and thereby allowing for a much more efficient use of resources. However, this circuit possesses high sensitivity to process and temperature variations. That been said, the simulations results presented here verify that the circuit operates within the confines of the specifications.

The layout design is critical for this type of power management circuits. The power transistor and the output current distribution metal paths should be placed and drawn conscientiously. The load regulation performance is deeply affected by the parasitic resistances that appear throughout the layout, to the extend of causing the schematic design stage coefficient to augment by a 100 times. Thus, the use of wide metal lines and a large amount of contacts and vias is necessary to ensure an accurate LDO.

Althought the active feedback compensation scheme is inherently sensitive to temperature variations, it yields a highly resilient steady-state performance towards the same phenomenon, as it can be observed in the temperature sweep analyses. Critical performance indicators such as preset output voltage at full-load condition, quiescent current, load regulation and line regulation displayed low temperature coefficients. Thus, the poly resistors used for temperature compensation were indeed a nice addition to the design.

The LDO overall performance when experiencing process and temperature varia-

tions was satisfactory. The quiescent current is kept under 60 μA, the PSRR remains below -40 dB at the 10 kHz frequency, all voltage spikes are kept under 200 mV, and the load transient settling times do not surpass 3 μs. Hence, it can be stated that the LDO topology proposed in this dissertation meets all specifications while maintaining the power consumption at a minimum. This, in turn, makes it suitable for low power SoC applications.

6.2 Future Work

Regarding the design of the LDO, it would be interesting to assess its performance using an NMOS instead of PMOS as the power transistor. NMOS transistors possess a higher transconductance and mobility than PMOS, which would result in smaller (die area) and faster LDO. However, the main issue to resolve is the voltage levels of its gate capacitance. Obviously, the dynamic range would have to be higher for the NMOS case, which might complicate the error amplifier design. Nevertheless, some research has been conducted on the subject and a viable solution has been proposed: a charge pump after the input supply in order to boost up the higher supply rail of the error amplifier and thus allow for a higher dynamic range at its output. Nevertheless, the extra circuitry and noise induced by the charge pump should be taken into consideration before stating that the proposal is indeed viable.

Another interesting idea, design-wise, is to make the voltage spike detection circuit through capacitive coupling adaptive and release the active feedback of this complicated task. This circuit creates a RHP zero in the frequency response, which could be use to track the pole associated with the output load. The adaptive feature could be incorporated with a variable resistor or a varactor. Furthermore, the transient behavior of the dynamic biasing technique will not be affected as long as the RC constant remains within a certain range.

Once the design and simulation steps are concluded, it is paramount to perform the measurements of the fabricated chips in order to verify the methodology and models used in this project.

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